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STANFORD UNIVERSITY · STANFORD, CA 94305

JSEP ANNUAL REPORT

1 May, 1988 through 30 June, 1989

James S. Harris, Jr.
JSEP Principal Investigator
and Program Director

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JSEP ANNUAL REPORT

Period of 1 May 1988 - 30 June 1989

Department of Electrical Engineering
Stanford University
Stanford, CA 94305

Joint Services Electronics Program
(U.S. Army, U.S. Navy and U.S. Air Force)
Contract DAAG-29-85-0048

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Abstract

This is the annual report of the research conducted at theStanford Electronics Laboratories underthe sponsorship of the Joint Services Electronics Program from 1 May 1988 through 30 June 1989. This report summarizes the area of research, identifies the most significant results and lists the dissertations and publications sponsored by the contract DAAG29-85-K-0048.

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JSEP ANNUAL REPORT

April 1, 1988 - June 30, 1989

Introduction

The JSEP contract supports a program of unclassified basic research in electronics conducted by faculty members of the Electrical Engineering Department of Stanford University as a component of the research program of the Stanford Electronics Laboratories. The Stanford Electronics Lab JSEP Director and Principal Investigator is Professor James Harris. He is responsible for the selection of the best individual proposals, coordination between Stanford and the JSEP TCC and coordination between the selected areas of the JSEP Program. In planning the JSEP Program at SEL, a general objective is to develop new projects with 3-6 years of JSEP sponsorship, leading to transition to DoD or other agency program funding. This report covers the first year of our current 3 year cycle. The two new projects supporting newly appointed faculty, John Cioffi and Bruce Wooley began in near the third year of the prior contract and are being carried forward in the current program during the next two years of the current contract. Thus, the projects remain those defined in our proposal. In addition, a new faculty member, Simon Wong, will be supported.

Two of the major program highlights realized during the past year are a result of being able to quickly switch JSEP funds onto new projects before other sources are available. These highlights are on high T_c superconductors. These highlights as well as two others are described below. Following these highlights, the specific objectives and progress in each work unit are reported.

The focus of the JSEP project on Molecular Beam Epitaixal (MBE) growth of high temperature superconductors is a strong collaboration with researchers at Varian Associates. The ability of MBE to grow in-situ layered, metastable $Bi_2Sr_2Ca_{n-1}Cu_nO_x$-like compounds has been demonstrated. This is a major step in the development of artificially layered combinations of perovskite-related compounds. A low growth temperature is required to grow such layered structures. Yet small free energy differences between the layers make this an elusive quest since layer imperfection can be "frozen in." Shuttered MBE growth is the most promising technique to achieve this custom layering ability.

Photoemission studies have been performed on single crystals of the high temperature superconductor $Bi_2Sr_2CaCu_2O_8$. We have obtained a wealth of information about the bulk electronic structure of the materials, in addition to the properties of the metal-

superconductor interface for a wide series of metals. In particular, Gold is especially inert, and is the most likely candidate for low resistance contacts.

Circuit design considerations and process integration issues have been investigated for the integration GaAs components on a silicon substrate with an integrated circuit. In particular, we have studied the integration of a GaAs photodetector on a silicon substrate containing the preamplifier for a fiber-optic receiver. The first functional, fully integrated, GaAs/Si receiver front-end has been successfully fabricated. This is the first reported integration of GaAs components and Si bipolar circuits.

We have demonstrated devices with lateral features of less than 100 nm that exhibited electrical characteristics that result from tunnelling between potential wells formed in a two-dimensional electron gas. More importantly, these devices were built in different configurations on the same substrate so that it was possible to compare the resonant tunnelling characteristics for different structures that imparted different degrees of confinement on the electrons. MODFETs were fabricated with a single gate, a dual gate, a dual gate with cross electrodes ("railway gate") and a single gate with cross electrodes. In particular for the highest degree of confinement, employing a two dimensional electrode structure, we observed increased oscillations in the transconductance.

The technical knowledge developed under the JSEP contract is widely disseminated through sponsor reviews, presentations of papers at technical meetings, publications in the open literature, discussions with visitors to the laboratories, and publication of laboratory technical reports.

Unit: 1

TITLE: Molecular Beam Epitaxy of High T_c Superconductors and Investigation of Quantum Well Structures

Principal Investigator: James S. Harris, Jr.

Research Associate: Eric S. Hellman

Graduate Students: Darrell G. Schlom, Zong Jian Chen and Peng Cheng

A. MOLECULAR BEAM EPITAXY OF HIGH T_c SUPERCONDUCTORS

1. Scientific Objectives:

The discovery of a class of materials which exhibit superconductivity at unprecedented temperatures has opened new possibilities for the future of electronic devices. The polycrystalline nature of the ceramic forms of these materials is likely to be unsuitable for electronics applications. In addition, the very short coherence lengths of these superconductors has made it difficult to prepare thin film tunnel junctions in the usual ways. The ideal form of these materials is thus likely to be that of epitaxial films, prepared in such a way that composition and structure can be controlled at the atomic layer level. The syntactic intergrowths of $Bi_2Sr_2Ca_{n-1}Cu_nO_{2n+4}$ or $Tl_2Ba_2Ca_{n-1}Cu_nO_{2n+4}$ phases where n ranges from 1 to 5 makes one wonder if this layering can be controlled on a layer by layer basis. Such layering might not only encompass the bismuth and thallium families of superconducting compounds, but also mixtures of any perovskite-related layers having compatible lattice geometries. If available, such a growth technique would be useful for device fabrication, would offer an unparalleled technique to fabricate metastable superlattice mixtures to test high T_c theories, and may allow the growth of higher temperature superconducting compounds once the proper theory is established. It is with these goals in mind that we have undertaken a systematic study of the growth of oxide compounds by molecular beam epitaxy (MBE).

2. Summary of Research:

The growth of fully oxidized compounds by MBE offers significant challenges compared to its conventional use in the growth of semiconductor compounds. Clearly to realize the described layered metastable structures, a low temperature, in-situ growth method is required. Further an activated species of oxygen is necessary to bring the constituent elements to the proper oxidation state while maintaining the long mean free path

necessary for MBE. Finally, composition control is crucial in order to repeatedly lay down exact "monolayers" of the desired composition. This report describes our progress related to the in-situ growth of layered $Bi_2Sr_2Ca_{n-1}Cu_nO_x$ compounds by MBE. The in-situ growth of layered metastable structures is demonstrated. The undesirable randomness that exists in our present layers and in layers grown by other techniques is discussed. The necessity for low growth temperature, activated oxygen species, and stringent composition control to achieve an in-situ MBE capability is argued.

The work described here is the product of a collaboration between the MBE groups at Stanford University and at Varian Research Center and the High T_c Thin Film group at Stanford. This work was initially supported by JSEP, Varian and NSF, respectively for each of the above groups. This early work has led to DARPA support of a joint Varian/Stanford MBE contract which will support a majority of the future work in this area.

The MBE system used for this work is a custom MBE machine, specifically designed at Varian for the growth of oxide superconductors and it is located at Varian Research Center in Palo Alto where all of the growths are carried out. A schematic of the growth chamber is shown in Fig. 1.1. Four conventional resistively heated MBE furnaces were used to provide fluxes of the constituents. Four independent shutters, controlled by a computer, were used to supply bursts of the separate metal constituents to the substrate. The growth was initiated on the substrate with a strontium layer, followed by copper, calcium, etc. ending the first half unit cell with bismuth. $Bi_2Sr_2Ca_{n-1}Cu_nO_x$ compounds with higher n were grown by lengthening the calcium and copper times accordingly. The shuttering sequence was repeated until the desired thickness was deposited.

A molecular oxygen source was used initially, however, we demonstrated that it does not provide sufficient oxidation under MBE growth conditions [Webb], [Hill]. Oxidation was first provided by a RF plasma source and later by an ozone source. During our work in the growth of $DyBa_2Cu_3O_{7-x}$ by MBE, we identified ozone as a potential oxidation gas for the MBE growth of cuprate superconductors [Hellman]. The ability of ozone to grow $YBa_2Cu_3O_{7-x}$ and $Bi_2Sr_2Ca_1Cu_2O_x$ under entirely MBE conditions (including substrate cooling after growth) was subsequently demonstrated [Berkley], [Maeda]. We use an ozone distillation technique to purify the ozone as shown in Fig. 1.1. This ozone system is similar to that used by other groups at Stanford to grow superconductors. The background pressures during growth were between $8x10^{-6}$ and $2x10^{-4}$ Torr.

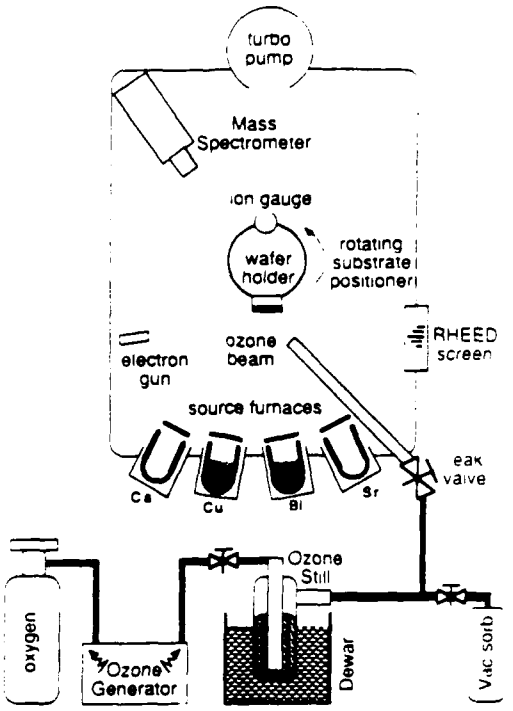

Figure 1.1 Schematic diagram of the MBE growth chamber.

During growth the crystal structure of the growing film was monitored using RHEED. After growth, the films were characterized by x-ray diffraction, RBS, electron microprobe, SEM, resistance versus temperature measurements, and cross-sectional transmission electron microscopy (XTEM). The x-ray measurements were made using a 4-circle diffractometer in the Bragg-Brentano geometry and radiation from a copper x-ray tube. The epitaxial relationships between the film and the substrate were investigated by making θ -2θ scans aligned to the substrate and scans of inclined film planes. The latter scans were used to obtain in-plane lattice constants and texture information.

The inability of molecular oxygen to form cuprate superconducting oxides in-situ under MBE conditions should be expected from thermodynamic considerations. Figure 1.2(a) shows the stability region for each of the binary oxide constituents that make up Bi-Sr-Ca-Cu-O compounds. On each reaction line both the products and reactants exist in equilibrium at a particular temperature and O_2 pressure. On the higher pressure and lower temperature side of the line (above the line), only the higher oxidation state will exist in equilibrium. Similarly on the lower pressure and higher temperature side of the line (below the line) only the lower oxidation state will exist in equilibrium. Of the desired oxidation states, Bi^{3+}, Sr^{2+}, Ca^{2+} and Cu^{2+}, the cupric oxidation state requires the highest oxygen pressure for the range of growth temperatures shown in Fig. 1.2(a).

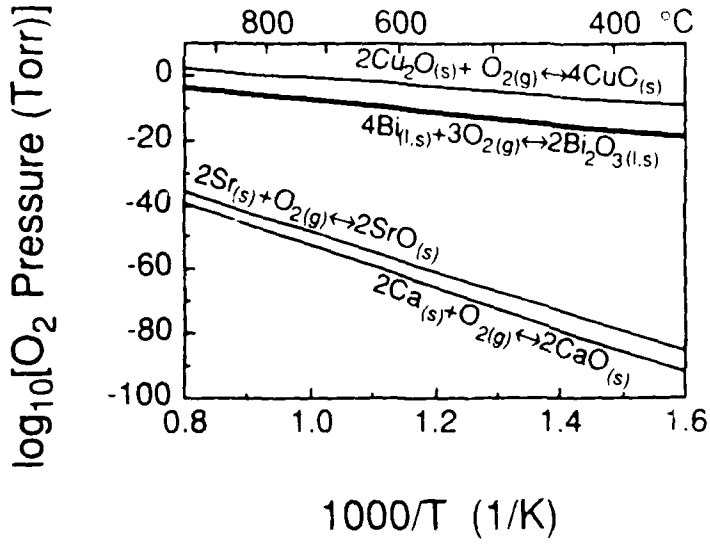

Figure 1.2(a) Lines of coexistence of the binary oxide constituents of Bi-Sr-Ca-Cu-O compounds as a function of O_2 pressure and reciprocal temperature. On each line both oxidation states exist in equilibrium. Above each line only the higher oxidation state exists, while below each line only the lower oxidation state exists. Calculated from thermodynamic data given in Ref. [JANAF] and Ref. [NB Mines].

The variation of the mean free path in oxygen together with the constituent oxide stability lines are shown in Fig. 1.2(b) for practical growth pressures. In order to be in the Knudsen (molecular flow) regime necessary for MBE, the mean free path must be longer than the source to substrate distance, about 20 cm. A 20 cm mean free path implies a maximum O_2 operating pressure of about 4×10^{-4} Torr. In order to be above the Cu^{2+} line, the growth temperature must be lower than 580°C. Further, compounds like $YBa_2Cu_3O_{6+x}$ require additional oxygen ($x>0.5$) to become superconducting. The corresponding lines for higher oxidation lie on the higher oxygen pressure side of the Cu^{2+} line. For example, to achieve $YBa_2Cu_3O_{6.5}$ for an oxygen pressure of 4×10^{-4} Torr, thermodynamics implies that a substrate temperature of less than 350°C must be used [Freitas], [Verweij]. To achieve $YBa_2Cu_3O_{6.9}$ at this same MBE compatible pressure, a substrate temperature less than about 250°C must be used [Verweij].

Such low substrate temperatures are clearly non-physical. Surface diffusion is likely insufficient for good crystallization since these temperatures lie far below the 550-700°C substrate temperature range used by most researchers to grow good in-situ superconducting cuprate films. At such low temperatures kinetic barriers will likely dominate as has been noted for the oxidation of bismuth by oxygen [Hill].

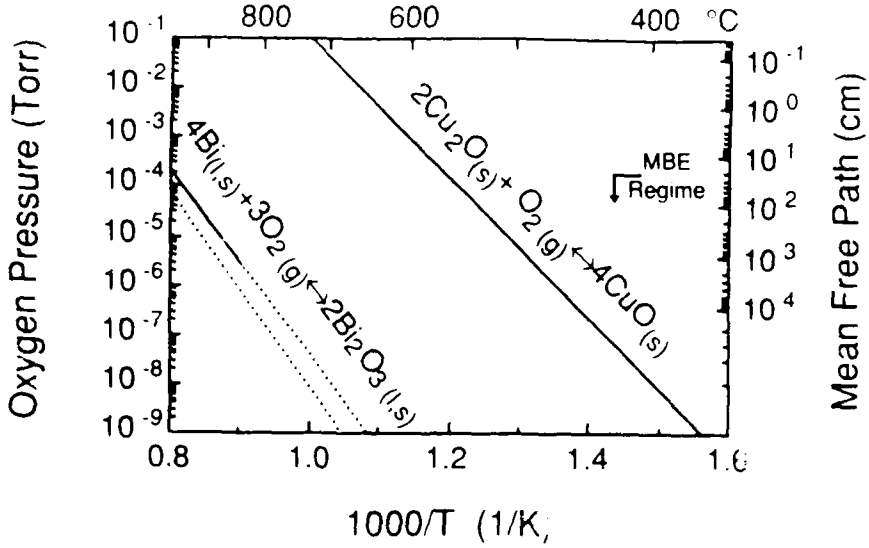

Figure 1.2(b) Oxygen pressure and corresponding mean free path at room temperature versus reciprocal temperature for the most difficult to oxidize species in (a). The dashed lines indicate extrapolated thermodynamic data from the temperature region where the given phases exist.

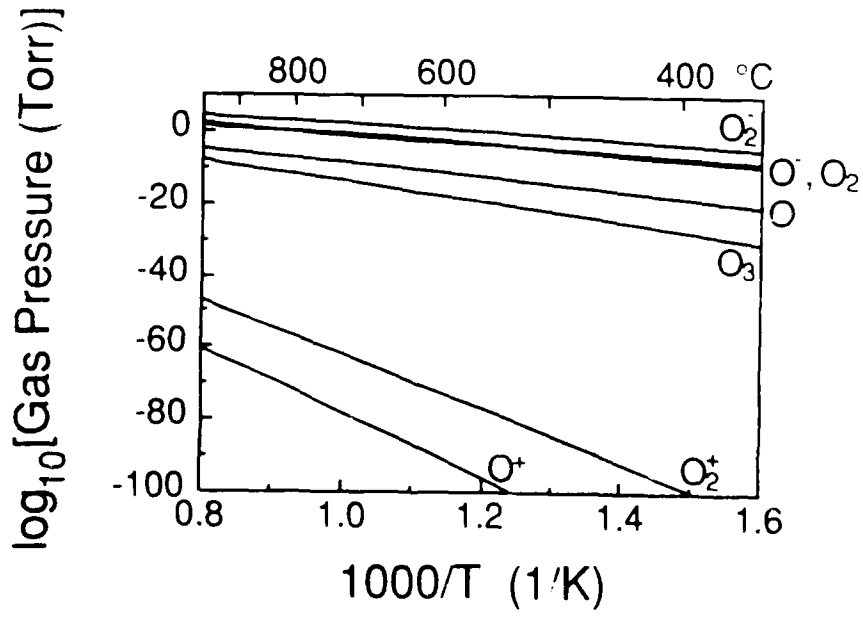

Figure 1.2(c) Lines of coexistence of Cu_2O and CuO with various gaseous oxidants as a function of oxidant pressure and reciprocal reaction temperature. Lines for the oxidants O, O^+, O^-, O_2, O_2^+, O_2^-, and O_3 are indicated. Calculated from thermodynamic data given in Ref. [JANAF].

A thermodynamic comparison of the ability of other oxygen species to oxidize copper is shown in Fig. 1.2(c). The $Cu_2O_{(s)} \leftrightarrow CuO_{(s)}$ coexistence line is shown as a function of oxygen species pressure and substrate temperature for O, O^+, O^-, O_2, O_2^+), O_2^-, and O_3. From a thermodynamic standpoint, O^+, O_2^+, and O_3 have the greatest oxidation ability. The pressure and temperature conditions necessary to achieve Cu^{2+} with these species will depend on the kinetics of their decomposition on the hot substrate. The oxidation ability of alternative non-equilibrium oxidants can be measured experimentally.

To get an idea of the conditions necessary to grow cuprate superconductors using ozone, the ability of ozone to oxidize copper was measured by depositing copper onto a substrate in the presence of ozone. X-ray diffraction indicated solely the presence of CuO in the films grown at room temperature and ozone background pressures down to 1×10^{-5} Torr. With the substrate at 600°C, only CuO was observed at background pressures down to 5×10^{-7} Torr. This indicates that ozone allows the growth of CuO at substrate pressures at least two orders of magnitude lower than when O_2 is used.

Figure 1.3 shows θ -2θ x-ray scans of several of our films. These films have lattice constants and 0 0 2ℓ reflection intensities resembling those of the bulk $Bi_2Sr_2Ca_{n-1}Cu_nO_{2n+4}$ (for n=1-3) phases. However, unlike the growth conditions for bulk phases, non-equilibrium conditions are likely present during the growth of these films. Diffusion in the growth direction is inhibited by the low growth temperature and by supplying the substrate with alternate bursts of the constituent metals. Hence, it is conceivable that the phases formed in these films are different from those formed in bulk samples formed under conditions far closer to equilibrium. Since we have not explicitly determined the structure and site occupancy of the phases in our films, yet find them similar to bulk phases, we refer to them as $Bi_2Sr_2Ca_{n-1}Cu_nO_x$-like phases. In Fig. 1.3 x-ray patterns of $Bi_2Sr_2Cu_1O_x$-, $Bi_2Sr_2Ca_1Cu_2O_x$-, $Bi_2Sr_2Ca_2Cu_3O_x$-, and $Bi_2Sr_2Ca_4Cu_5O_x$-like phases are shown.

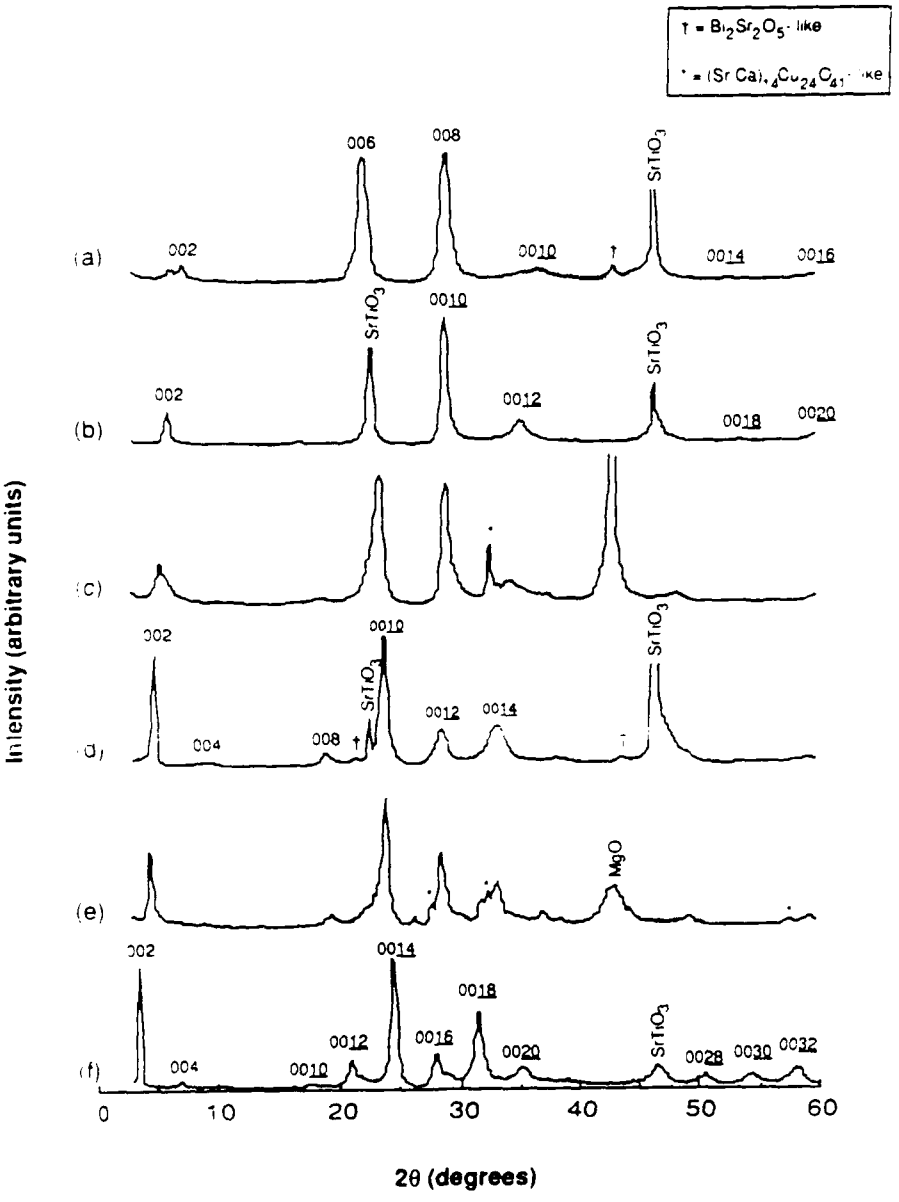

Figure 1.3 θ-2θ x-ray scans of as-grown films containing aligned $Bi_2Sr_2Ca_{n-1}Cu_nO_x$-like phases. 0 0 2ℓ indices are given for the $Bi_2Sr_2Ca_{n-1}Cu_nO_x$-like phase peaks. Peaks due to impurity phases are also labeled. (a) $Bi_2Sr_2Cu_1O_x$-like, rocked 0.5 degrees in omega off alignment to the $SrTiO_3$ {100} substrate. Grown at T_{sub}≈550°C and $PO_{3,Background}$≈3x10-5 Torr. (b) $Bi_2Sr_2Ca_1Cu_2O_x$-like, rocked 0.5 degrees in omega off alignment to the $SrTiO_3$ {100} substrate. Grown at T_{sub}≈600°C and $PO_{3,Background}$≈2x10-5 Torr. (c) Observed θ-2θ x-ray scans of as-grown film. Peaks due to impurity phases are labeled. Rocked 0.5 degrees in omega off alignment to the MgO {100} substrate. Grown at T_{sub}≈600°C and $PO_{3,Background}$≈3x10-5 Torr. (d) $Bi_2Sr_2Ca_2Cu_3O_x$-like, rocked 0.5 degrees in omega off alignment to the $SrTiO_3$ {100} substrate. Grown at T_{sub}≈590°C and $PO_{2\ Plasma,Background}$≈2x10-5 Torr. (e) Observed θ-2θ x-ray scans of as-grown film. Peaks due to impurity phases are labeled. Rocked 1 degree in omega off alignment to the MgO {100} substrate. Grown at T_{sub}≈600°C and $PO_{3,Background}$≈1x10-5 Torr. (f) $Bi_2Sr_2Ca_4Cu_5O_x$-like, rocked 1 degree in omega off alignment to the $SrTiO_3$ {100} substrate. Grown at T_{sub}≈580°C and $PO_{2\ Plasma,Background}$≈8x10-6 Torr.

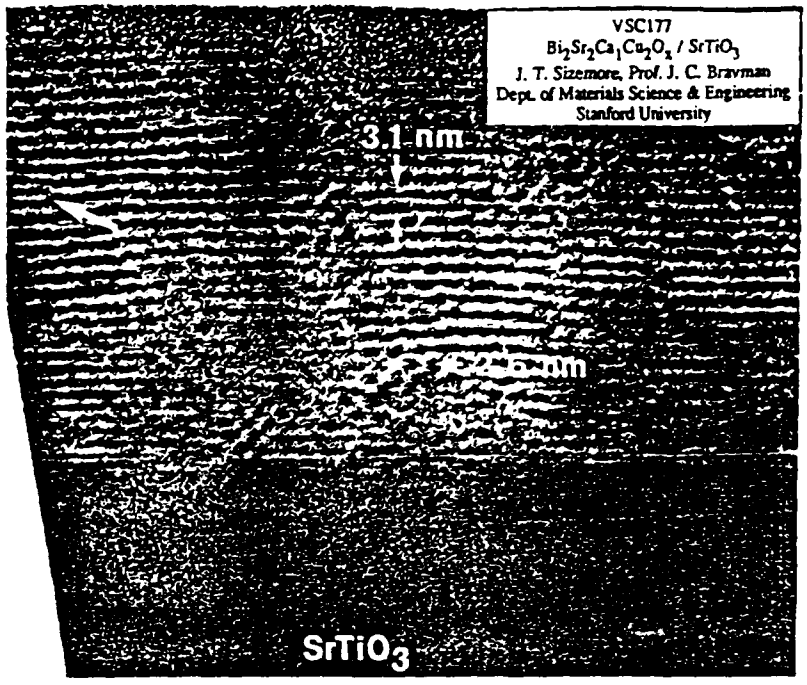

Figure 1.4 Cross-sectional TEM image of an as-grown $Bi_2Sr_2Ca_1Cu_2O_x$-like sample grown on $SrTiO_3$ (001). The electron beam is incident along the [110] $SrTiO_3$ zone axis. Grown at T_{sub}≈560°C and $P_{O_2\ Plasma,Background}$≈2x10^{-4} Torr.

A cross-sectional TEM image showing the interface region between the $SrTiO_3$ substrate and a $Bi_2Sr_2Ca_1Cu_2O_x$-like film is shown in Fig. 1.4. The registry between the substrate and epitaxial layer is evident. The ≈15 Å fringe spacing in the direction of growth is consistent with the growth of a c-axis oriented $Bi_2Sr_2Ca_1Cu_2O_x$-like film. Further, the lateral ≈26 Å periodicity present in places shows the b-axis superstructure observed in bulk $Bi_2Sr_2Ca_1Cu_2O_8$ samples [Marshall]. Note that the a-axis and b-axis are reversed in adjacent regions. This is not surprising since the a and b axes are very close in length and the film was grown on a cubic substrate with a square surface net. The presence of a stacking fault is indicated by the arrow in Fig. 1.4.

Figure 1.5 shows a cross-sectional TEM image of a $Bi_2Sr_2Ca_4Cu_5O_x$-like film. The ≈25 Å fringe spacing along the growth direction is consistent with the growth of a c-axis oriented film of this phase. Although as many as five CuO_2 layers have been seen between BiO layers in regions of bulk compounds, a structure with the long range regularity seen in this TEM photo and evidenced by the x-ray of Fig. 1.3(f) has not been produced by bulk methods. The inability of bulk methods to produce a well ordered $Bi_2Sr_2Ca_4Cu_5O_{14}$ phase is believed to be due to the small free energy differences between the phases in the bismuth $Bi_2Sr_2Ca_{n-1}Cu_nO_{2n+4}$ family [Tarascon]. The fact that we have grown a nearly single phase $Bi_2Sr_2Ca_4Cu_5O_x$-like layer indicates the ability of the MBE growth technique to produce metastable layered $Bi_2Sr_2Ca_{n-1}Cu_nO_x$-like compounds.

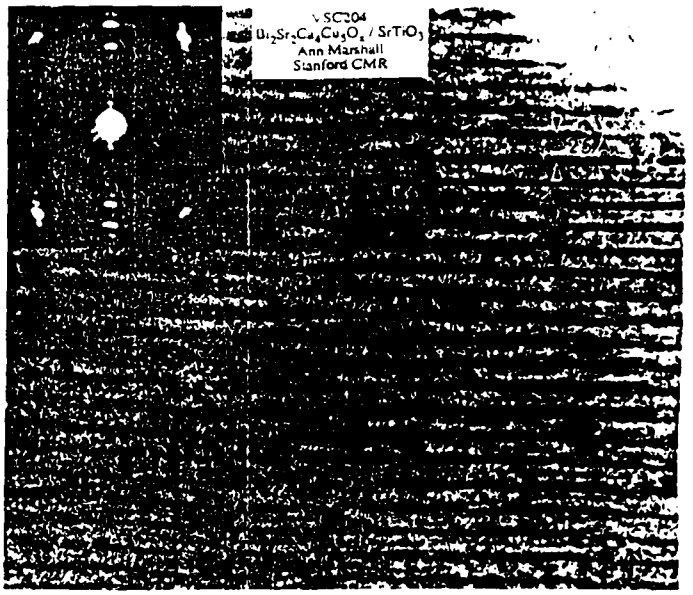

Figure 1.5 Cross-sectional TEM image of an annealed $Bi_2Sr_2Ca_4Cu_5O_x$-like sample grown on $SrTiO_3$ (001). The four hour 550°C oxygen anneal did not significantly alter the q-2q x-ray pattern or the semiconducting r vs. T curve of this sample. Grown at $T_{sub} \approx 580°C$ and $P_{O_2\ Plasma,Background} \approx 8 \times 10^{-6}$ Torr.

The intensity of the RHEED pattern is observed to oscillate during the growth of some films. Somewhat similar oscillations were seen in the MBE shuttered growth of Dy-Ba-Cu-O compounds [Schlom]. Although it is not surprising that the period of the oscillation corresponds to that of the shuttering, the non-monotonic shape is interesting. We do not have an explanation for the observed oscillation shape.

Several of our films, including the one just described, have exhibited unusual x-ray patterns. Although their long c-axis lengths and peak intensity distributions are similar to the $Bi_2Sr_2Ca_{n-1}Cu_nO_{2n+4}$ phases, it is not possible to index their peak positions to any of the known $Bi_2Sr_2Ca_{n-1}Cu_nO_{2n+4}$ phases. Two examples are shown in Fig. 1.3(c) and Fig. 1.3(e). A least squares estimate of the c-axis length based on the peak positions results in ≈34 Å and ≈40.5 Å c-axis lengths for these two patterns. Not only are these lengths far from the known $Bi_2Sr_2Ca_{n-1}Cu_nO_{2n+4}$ phases (24.6 Å, 30.8 Å, 37.1 Å, . . .), but indexing the peaks to these intermediate lattice constants requires the use of both even and odd 00l peaks. Odd 00l x-ray diffraction peaks are forbidden in the known $Bi_2Sr_2Ca_{n-1}Cu_nO_{2n+4}$ phases since they all contain a glide plane half way up the unit cell. Similar unexplained x-ray patterns have been seen by other researchers in films grown by sputtering, [Kojima] shuttered ion beam sputtering, [Fujita] and laser ablation [German]. We have investigated whether these patterns are due to a new ordered structure or to the disordered random layering of mixtures of the known $Bi_2Sr_2Ca_{n-1}Cu_nO_{2n+4}$ phases.

The x-ray pattern for mixtures of randomly stacked $Bi_2Sr_2Ca_2Cu_3O_{10}$ and $Bi_2Sr_2Ca_3Cu_4O_{12}$ layers was calculated using the theory of Hendricks and Teller [Hendricks]. Comparison of the observed x-ray spectra with the calculated x-ray spectra leads us to conclude that the observed x-ray spectra is more consistent with random layering than with a new ordered structure. Cross-sectional TEM was used to further investigate the layered nature of these unusual samples. We conclude that the unusual x-ray patterns observed so far by ourselves and others are due to random layering. A similar hypothesis was put forward by [Fujita] et al.

In conclusion, the ability of MBE to grow layered metastable $Bi_2Sr_2Ca_{n-1}Cu_nO_x$-like compounds in situ is demonstrated. This is a major step in the development of a growth method capable of tailor-making layered combinations of perovskite-related compounds. A low growth temperature is required to grow such layered structures. Yet small free energy differences between the layers make this an elusive quest since layer imperfection can be "frozen in." Shuttered MBE growth is a likely technique to achieve this custom layering ability, provided stringent composition control can be maintained on an atomic layer by atomic layer scale. This control is not nearly as important in growth at high temperatures where diffusion is sufficient to allow the phase separation of equilibrium structures. Thus it is seen that the "freezing in" of metastable layerings at low temperature is both an advantage in allowing new layerings to be grown and a disadvantage in that poor layering control can lead to layering disorder.

B. INVESTIGATION OF QUANTUM WELL STRUCTURES

1. Scientific Objectives

The objective of this project is to investigate heterojunction, quantum well and superlattice concepts and their application to new electronic devices with superior performance to devices based upon current semiconductor device principles. The small vertical dimensions which can now be readily achieved by Molecular Beam Epitaxy (MBE) make it possible to fabricate quantum well structures which are totally dominated by quantum mechanical effects. The properties of electron transport and storage in various regions of these quantum well structures are not well understood and their application to an entirely new generation of electron devices is in its infancy. The long range goal is to create lateral quantum size dimensions to examine quantum wires and dots. The project will initially focus on the effects of doping on the electron transport in resonant tunneling diodes and new designs of double barrier resonant tunneling diodes to improve peak to valley current ratio and peak current density.

2. Summary of Research

Resonant tunneling has been intensively studied in recent years [Tsu], [Chang], [Sollner] and [Reed]. Much of the early research has focused on improving the characteristics of RTDs. Peak-to-Valley Ratio and peak current density are two of the most important characteristics of RTDs because they determine the switching speed of RTD devices. RTDs also provide us a macroscopic method to study quantum mechanical phenomena because the carrier transport in RTDs is dominated by quantum transport. Current resonant tunneling models ignore effects of accumulation layers, spacers, etc., in the cathode region. We have focused initial efforts on understanding the role of the cathode region and its role in optimizing device design.

The characteristics of resonant tunneling diodes are strongly affected by the doping profile of the structures. [Muto] et al, did a systematic study on Si doping profiles in double barrier resonant tunneling diodes (DBRTDs) and found that the peak-to-valley current ratio (PVCR) increased as the spacer layer thickness increased. Recently, [Huang] et al, applied two step spacer layers to get an even higher PVCR. They observed PVCR values as high as 21.7 at 77°K in AlGaAs/GaAs DBRTDs which they attributed to better material quality (few background impurity density). However, [Wolak] et al, studied the effects of doping in the GaAs well in AlGaAs/GaAs DBRTDs and found that the effects of ionized impurities were not strong.

We studied the effects of Si doping in the AlAs barrier layers of AlAs/GaAs/AlAs DBRTDs. Three samples were grown on semi-insulating GaAs (100) substrates by molecular beam epitaxy at 600°C in a Varian Gen II system. The AlAs/GaAs/AlAs DBRTDs were grown on top of a one micron $2x10^{18}$ cm^{-3} Si doped buffer layer. Two step spacer layers were used on both sides of the AlAs/GaAs/AlAs active region. The thickness of the first spacer is 500Å. The doping was graded from $2x10^{18}$ cm^{-3} to $2x10^{16}$ cm^{-3} within the first 100Å and maintained constant through the remaining 400Å. The second spacer layer is 25Å thick and undoped. The thickness of both AlAs barriers is 25Å. The GaAs well width is 50Å. The doping level in the central 15Å of both AlAs barrier is varied. In sample A, the barriers are undoped. In sample B, both barriers are doped to $1.2x10^{17}$ cm^{-3}. In sample C, the top AlAs barrier is undoped, while the bottom AlAs barrier is doped to $3x10^{18}$ cm^{-3}. The remainder of the barriers and the well are undoped. The top contact layer is 5000Å and doped to $2x10^{18}cm^{-3}$ with Si. The structures and doping profiles of the samples are shown in Figure 1.6.

Current-Voltage (I-V) characteristics were measured at both 300K and 77K. The I-V characteristics are very similar in both bias directions. Even with asymmetrical doping in the AlAs layers in sample C, no significant difference in the I-V characteristics were

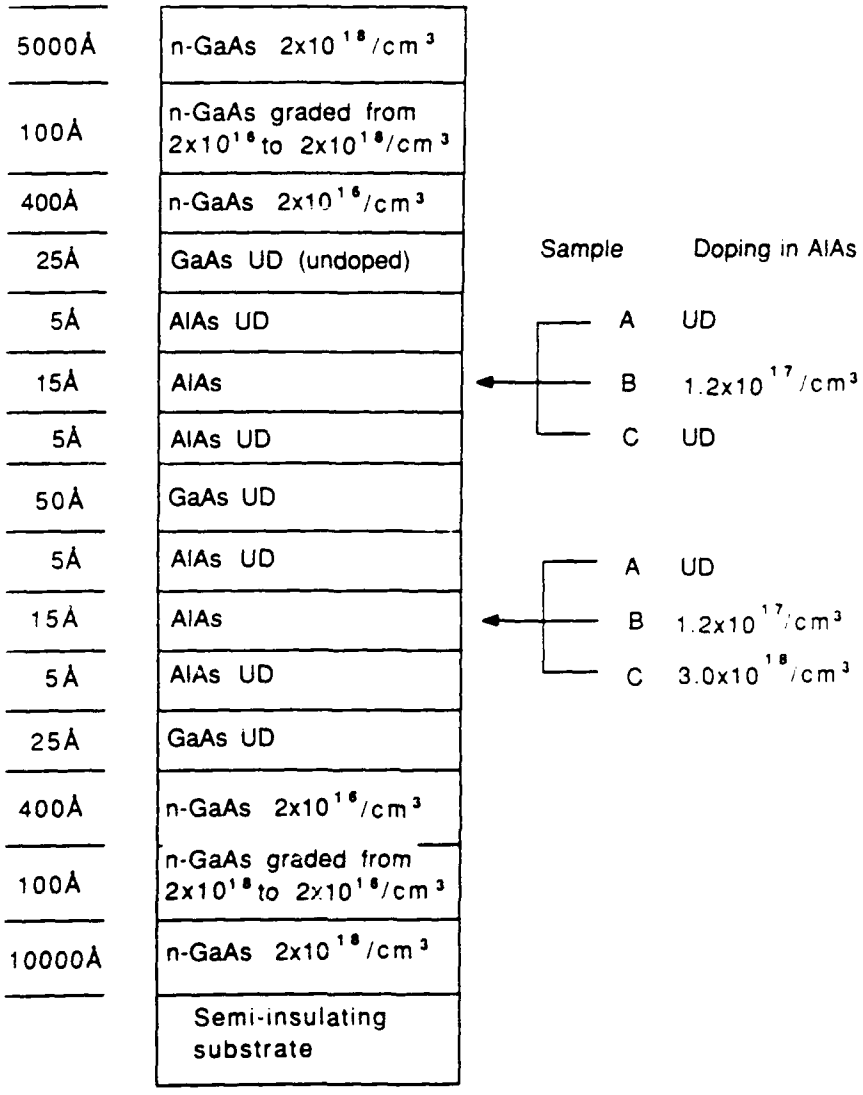

Figure 1.6 Structures of Sample A, B and C.

observed between the forward and reverse bias direction. This indicates that the effect of the Si doping in the front barrier and rear barrier are similar when the doping level is as high as $3x10^{18}$ cm^{-3}. Values of PVCR as high as 3.5 were observed in both samples A and B. Even in sample C, with $3x10^{18}$ cm^{-3} Si doping in the bottom AlAs barrier, a very reasonable average PVCR of 2.4 was observed. The peak and valley voltages both decrease as the doping in the AlAs barrier increases. The peak currents of samples A, B and C are very similar. The valley currents of samples A and B are also very similar, while the valley current of sample C is significantly larger. The difference between the peak and valley currents decreases as the doping in the AlAs barrier increases. Measurement at 77°K yielded maximum values of PVCR of 11.3, 11.3 and 8.2 on samples A, B and C, respectively.

Since a doping level of $1.2x10^{17}cm^{-3}$ inside the AlAs barriers has virtually no effect on the resonant tunneling characteristic, reduced impurity concentration in the active region of DBRTDs with two step spacer layers is not the main reason for the improvement in PVCR in this type of DBRTD vs. a standard, single spacer DBRTD. We believe that the band bending in the cathode side spacer layer forms a quasi barrier and this is the reason of the improvement of PVCR.

To further investigate the cathode region, we have investigated the effects of placing an AlGaAs chair barrier in front of the AlAs tunneling barrier in DBRTDs. The motivation for this study is to enhance aspects of transport in RTDs that are not included in many ballistic models which neglect dissipative mechanisms. While these relatively simple ballistic models are able to predict the general shape of RTD curves, they cannot accurately determine the characteristics in the negative differential conductance region. Precise knowledge of these characteristics is important for applications of RTDs.

One of the complications is that the bands are not flat in the cathode. Depending on the exact doping profile, the bands may bend up in large spacer regions as well as form an accumulation layer just before the double barriers. As we have pointed out in the Si doping effects experiment above, we believe that the cathode band profile is very important in determining the performance of RTDs. The chair barrier structure is designed to reduce the tunneling current from the accumulation layer in front of the tunneling barrier. Two samples were grown on n+ GaAs (100) substrates by molecular beam epitaxy. In sample D, the AlAs/GaAs/AlAs DBRTDs were grown on top of a 5000Å $2x10^{18}$ cm^{-3} Si doped buffer layer. Two step spacer layers were used on both sides of the AlAs/GaAs/AlAs active region. The thickness of the first spacer is 500Å. The doping was graded from $2x10^{18}$ cm^{-3} to $2x10^{16}$ cm^{-3} within the first 100Å and maintained constant through the remaining 400Å. The second spacer layer is 25Å thick and undoped. The thickness of both AlAs barriers is 20Å. The GaAs well width is 50Å. The barriers and the well are undoped. The top contact layer is 5000Å and doped to $2x10^{18}$ cm^{-3} with Si. In sample E, an undoped 4 monolayer AlGaAs (x=0.14, where x is Al content) chair barrier were grown before the growth of the AlAs/GaAs/AlAs double barrier structure. The rest of the structure of sample E is the same as that of sample A. The structures and doping profiles of the samples are shown in Fig. 1.7.

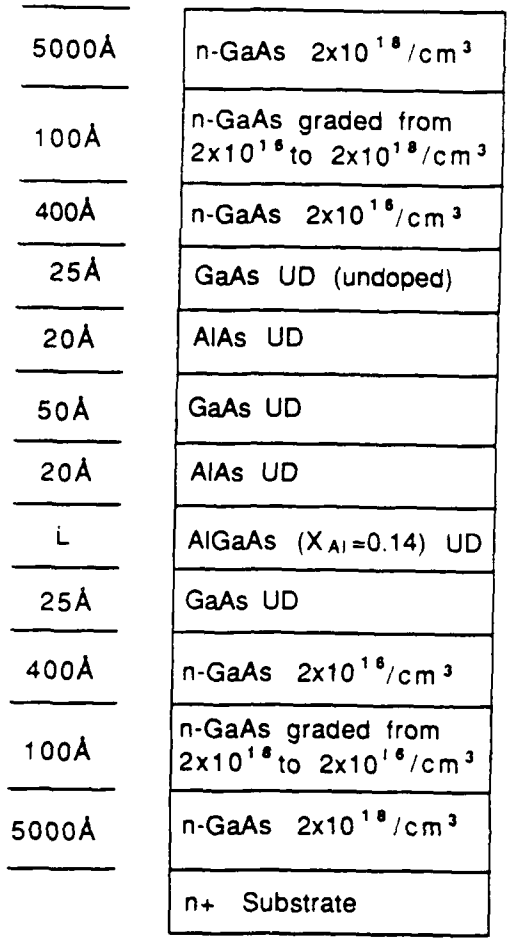

Figure 1.7 Structure of Sample D and E. There is no chair barrier in Sample D, L=0. There is a chair barrier in Sample E, L=4 monolayer.

In sample D, the room temperature PVCR is 4.2 in both bias directions. In sample E, the room temperature PVCR is 5.1 when the chair is on cathode side and only 3.7 when the chair barrier is on anode side. The PVCR of 5.1 is the best PVCR to date achieved in DBRTDs at room temperature. In sample E, when the chair barrier is on cathode side, the valley current is only about 40% of the valley current when the chair barrier is on anode side. This indicates that the chair barrier does reduce the valley current sufficiently when it is on cathode side. We believe that most of the current reduced by the chair barrier is tunneling from the accumulation layer in front of the tunneling barrier. Further improvement in PVCR and peak current density can be expected by using thinner AlAs barriers and optimizing the height and thickness of the chair barrier.

We have also investigated the effects of placing pseudomorphic InGaAs wells in the cathode of resonant tunnel diodes. We altered the spacer layers by including InGaAs wells

outside the barriers. As a result we have dramatically increased the peak current of the devices with a proportionally smaller increase in the valley current. These experiments have produced exceptional devices in addition to contributing to our understanding of the more subtle mechanisms involved in electron transport in these structures.

The structures used in our experiments had two 20Å AlAs barriers separated by 47Å of GaAs. The electrode doping was $2x10^{18}$ in the regions outside the spacer layers. On the anode side, a simple 100Å undoped GaAs spacer was used. On the cathode side, there was first a 100Å of $1x10^{17}$ silicon doped GaAs followed by 70Å of undoped material next to the barrier. We grew four different structures for this undoped region. In the first sample, the entire 70Å was GaAs. In the remaining samples 25Å, 45Å, or 65Å of the GaAs nearest the barrier was replaced with $In_{0.15}Ga_{0.85}As$. Thus an InGaAs quantum well was formed just outside the barrier.

When the devices were biased so that electrons were injected from the side with the InGaAs quantum well, the peak current of the 25Å InGaAs well device was about 2 times greater than the current of devices without an InGaAs well. The 45Å and 65Å InGaAs well devices had about 3.5 times higher peak current than the devices without InGaAs wells. The increased peak current density of these devices should increase their switching speed. The 45Å devices have peak current densities of 10^{-5} A/cm^2 concurrent with peak-to-valley ratios of greater than 5 at room temperature. Further improvement can be expected with thinner AlAs barriers and optimized InGaAs well configurations. The similarity of the reverse characteristics of all devices show that the barrier and well structures were not substantially altered by the preceding growth of the InGaAs well. Thus the changes in the characteristics can be attributed to the effect of the InGaAs well on the electron supply function. Experiments are in progress to determine the mechanism for the increased peak currents.

JSEP SUPPORTED PUBLICATIONS

1. J. S. Harris, Jr., J. N. Eckstein, E. S. Hellman, and D. G. Schlom, "MBE Growth of High Critical Temperature Superconductors," *J. Crystal Growth* **95**, 607 (1989).
2. J. N. Eckstein, D. G. Schlom, E. S. Hellman, K. E. von Dessonneck, Z. J. Chen, C. Webb, F. Turner, J. S. Harris, Jr., M. R. Beasley, and T. H. Geballe, "Epitaxial Growth of High-Temperature Superconducting Thin Films," *J. Vac. Sci. Technol.* **B7**, 319 (1989).
3. J. N. Eckstein, J. S. Harris, Jr., D. G. Schlom, I. Bozovic, K. E. von Dessonneck, and Z. J. Chen, "Development of Molecular Beam Epitaxial Growth of High Temperature Superconducting Compounds," Proceedings, *International Superconductivity Electronics Conference*, Tokyo (June 1989).
4. D. G. Schlom, A. F. Marshall, J. T. Sizemore, Z. J. Chen, J. N. Eckstein, I.

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5. P. C. Cheng, B-G. Park, S-D. Kim, and J. S. Harris, Jr., "The X-valley transport in GaAs/AlAs triple barrier structures", *J. Appl. Phys.* **65**, 5199 (1989).
6. P. Cheng and J. S. Harris, Jr., "Effect of Si doping in AlAs barrier layers of AlAs-GaAs-AlAs double-barrier resonant tunneling diodes", *Appl. Phys. Lett.* **55**, 572 (1989).

JSEP SUPPORTED PRESENTATIONS

7. J. S. Harris, Jr., J. N. Eckstein, E. S. Hellman, and D. G. Schlom, "MBE Growth of High Critical Temperature Superconductors," invited talk presented at the 5th International Conference on Molecular Beam Epitaxy, Sapporo, Japan, 8/88.
8. J. N. Eckstein, D. G. Schlom, E. S. Hellman, K. E. von Dessonneck, Z. J. Chen, C. Webb, F. Turner, J. S. Harris, Jr., M. R. Beasley, and T. H. Geballe, "Epitaxial Growth of High-Temperature Superconducting Thin Films," presented at the 9th Workshop on Molecular Beam Epitaxy, Purdue, 9/88.
9. J. N. Eckstein, J. S. Harris, Jr., D. G. Schlom, I. Bozovic, K. E. von Dessonneck, and Z. J. Chen, "Development of Molecular Beam Epitaxial Growth of High Temperature Superconducting Compounds," Proceedings, *International Superconductivity Electronics Conference*, Tokyo (June 1989).
10. D. G. Schlom, J. N. Eckstein, K. E. von Dessonneck, Z. J. Chen, I. Bozovic, J. T. Sizemore, C. Webb, F. Turner, J. S. Harris, Jr., J. C. Bravman, M. R. Beasley, and T. H. Geballe, "Molecular Beam Epitaxy of Layered Bi-Sr-Ca-Cu-O Compounds," presented at the Spring Meeting of the Materials Reseach Society, San Diego, 4/89.
11. P. Cheng and J. S. Harris, Jr., "Effect of Si doping in AlAs barrier layers of AlAs-GaAs-AlAs double-barrier resonant tunneling diodes", at the American Physical Society March meeting, St. Louis, 1989.

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Unit: 2

TITLE: Physics and Applications of Ultra-Small, High-Temperature Superconductors

SENIOR INVESTIGATORS: R. F. W. Pease and S. Y. Chou

RESEARCH STUDENTS: B. Boyer and D. R. Allee

Scientific Objectives

The overall objectives of this program are to investigate opportunities for new devices whose operation depends on quantum mechanical effects associated with the ultra-small nature of these devices. Obviously we hope to realize device concepts that promise superior performance than that achieved by devices based on current principles. Even if that desirable end is not realized we should in any case be in a position to optimize the design of devices employing lateral features below 100 nm when our ability to fabricate them moves from the laboratory to the manufacturing facility. During the last year we have had two specific objectives:

1. Investigate the physics and engineering of 3-5 compound semiconductor devices employing lateral features in the sub-100 nm size range and vertical dimensions below 10 nm. The small vertical dimensions that can can now be readily achieved with molecular beam epitaxy (MBE) make it possible to fabricate superlattice structures that are dominated by quantum size effects [Esaki 1970], [Esaki 1974] and [Sollner 1983]. The long mean free path of of the confined electrons in these structures makes it possible to fabricate structures with a periodicity that is much less than the mean free path [Warren]. The properties of carrier transport and storage in various regions of these ultra-small, three-dimensionally confined structures are not well understood and their application to an entirely new generation of electron devices is still in its infancy.

2. Extend the above investigation to the physics and engineering of devices not only exhibiting sub-100 nm lateral features but also employing high T_c superconducting materials. This was stimulated not only by the original discovery of such materials but by more recent successes in preparing thin (20 nm) films of high quality material. These films exhibit a high degree of anisotropy which renders unsatisfactory many traditional techniques for fabricating devices based on weak links. However recent advances in nanofabrication that have demonstrated features below 10 nm (under special circumstances features less than 2 nm have been demonstrated) raise the

possibility of being able to fashion, in thin film electrodes, lateral gaps that are of the order of a coherence length. Some related aspects are being proposed to AFOSR under a joint proposal with the Ginzton Laboratory (Geballe and Kapitulnik).

Progress

1. Ultra-small Lateral Quantum-Well Devices

Very significant progress has been made. The procedures for fabricating and testing such devices were developed to the point where a variety of different device structures were fabricated on a single substrate to allow accurate comparison between devices. Among the advances made were improvements in the electron beam resist processing and the subsequent lift-off steps and in mounting and making electrical contact for testing the devices at 4.2K. The following devices were successfully designed fabricated and tested:

1. A dual-gate lateral resonant-tunneling field-effect transistor (LARTFET) that employs two gate electrodes 80 nm wide separated by 100 nm (Fig. 2.1a). The electron transport is across the electrode structure. The substrate is semi-insulating GaAs with an 8-cycle superlattice (AlGaAS/GaAs) followed by a 500 nm buffer layer of GaAs. On top of this are deposited 2.5 nm undoped AlGaAs, 45 nm doped AlGaAs, and then a 50 nm n+ GaAS capping layer. Ohmic contacts are Au/Ge/Ni/Au patterned by optical lithography and lift-off and annealed at 450°C for 30 mins. Isolation is accomplished by two-stage Argon ion implant. The gate metal is patterned by 40 kV exposure of 70 nm thick Poly(methyl methacrylate) (PMMA) resist followed by lift off of 15 nm layers of Ti and Au. The two gates are biassed to induce an electric potential distribution in the 2D electron gas that results in a double barrier between source and drain (Fig. 2.1b).

2. A single-gate MODFET built on the same substrate to act as a control device. Testing of both devices involved measuring source-to-drain current as functions of gate voltage and of drain voltage with no illumination of the devices. Some results for drain current, I, vs. Gate voltage, Vgs, are shown in Figs. 2.2a and 2.2b for the single gate device and the dual gate device respectively. At room temperature both curves are smooth but at 4.2 K the curve for the dual gate device exhibits an oscillation in its slope which can be displayed as an oscillation in the value of transconductance gm while the control device exhibits no such conductance oscillation. The appearance of one cycle of conductance oscillation is consistent with resonant tunneling to the first bound state although there are many quasi-bound energy states in the lateral quantum well. As the gate voltage becomes less negative the energy separations decrease and hence the resulting departures from classical behavior are less marked. The transconductance fluctuation also disappeared

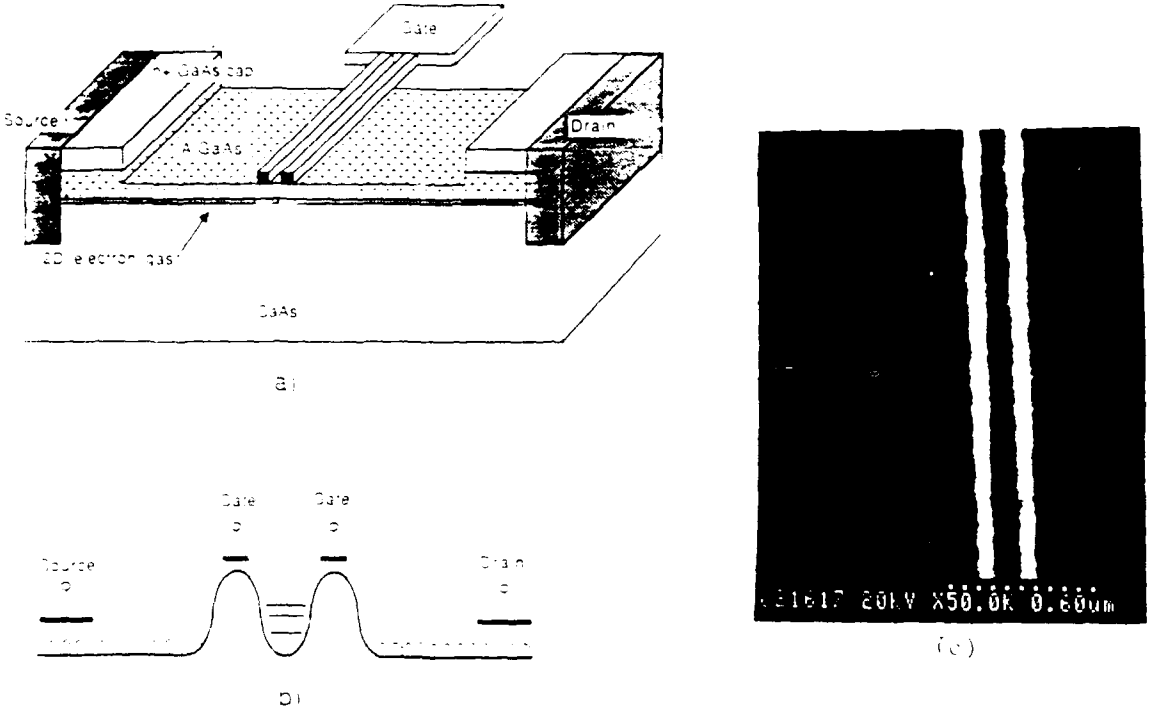

Figure 2.1(a) Schematic of a lateral resonant tunneling field-effect transistor which has dual closed placed fine finger gates instead of a single gate, (b) schematic of energy band diagram for the device. (c) scanning electron micrograph of gate structure.

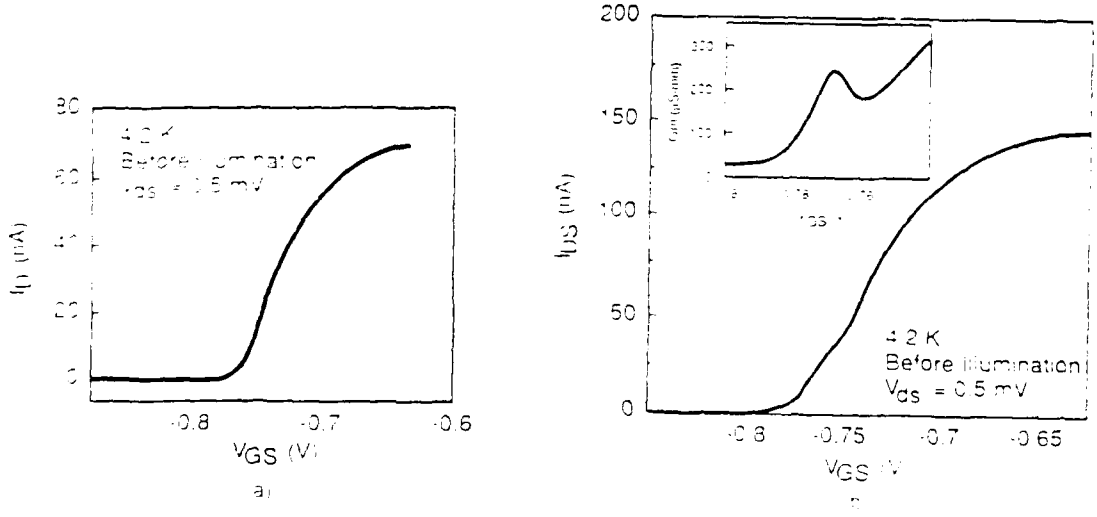

Figure 2.2 The drain current vs. the gate voltage at a fixed source drain voltage of 0.5 mV at 4.2K before illimination (a) for the single-80nm-gate MODFET exhibiting a smooth turn-on, (b) for a dual-80nm-gate LARTFET as a function of the drain voltage at a fixed source-drain voltage at 1 mV, exhibiting a foot and a shoulder.

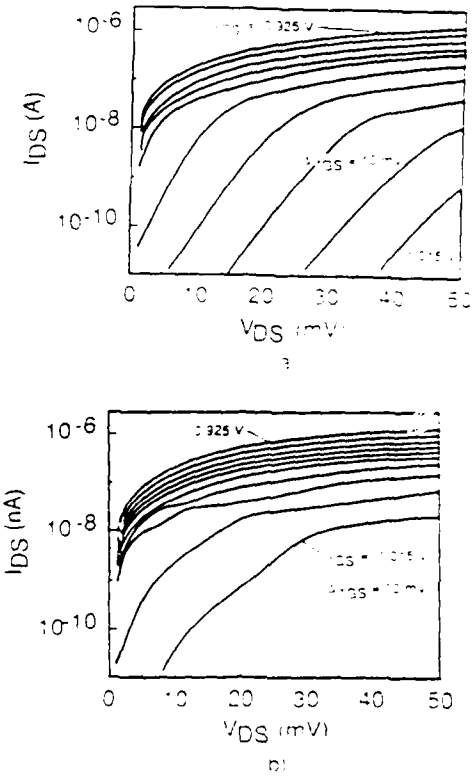

Figure 2.3 Logarithmical plot of drain current vs. the source-drain voltage at different gate voltages at 4.2K (a) for a single-80nm-gate FET, (b) for a dual-80nm-gate LARTFET.

when the drain voltage exceeded 5 mV which can be explained by the increased temperature of the electrons at higher drain voltages. In a second set of tests, drain current, Ids, was measured as function of drain voltage, Vds, for values of gate voltage, Vgs, close to the threshold value (Fig. 2.3). The curves for the LARTFET again show a conductance oscillation as opposed to the curves for the MODFET which show only one knee consistent with the presence of resonant tunneling through the double barrier structure. At higher values of Vgs the oscillation moves to lower values of Vds; this is consistent with the lower height of the barriers at less negative gate voltages requiring less drain voltage to move the energy levels in the well to the resonant condition.

When the devices had been illuminated the threshold voltages become more negative and remain that way for about 1 hour. More surprisingly additional conduction oscillations appear (Fig. 2.4). These appear for the MODFET control device which shows two peaks as opposed to the LARTFET which shows two. We speculate that the two additional peaks arise from trap states that become active when photons release the trapped electrons. In a further set of experiments on devices made with a thicker AlGaAs spacer layer (7 nm as opposed to 2.5 nm) the additional peaks disappeared.

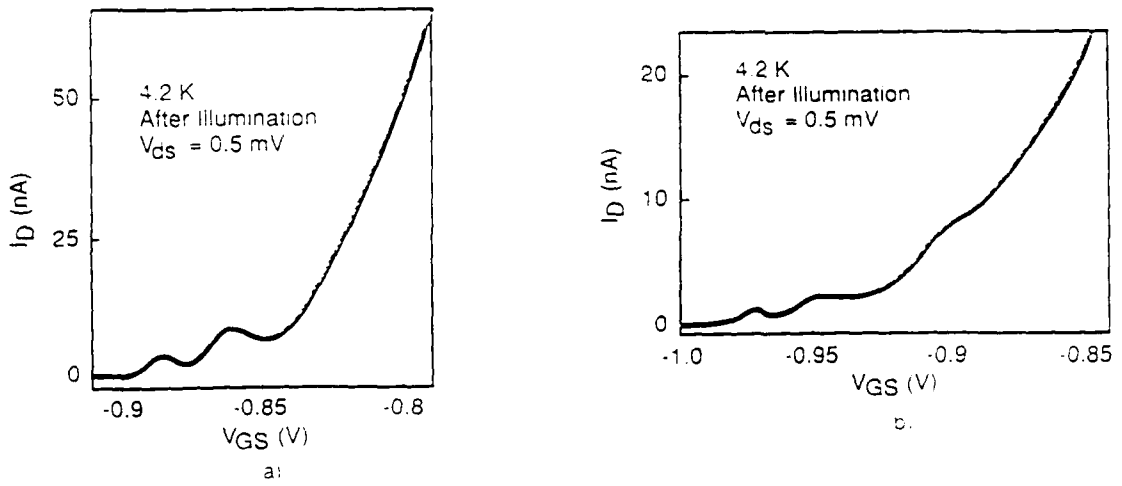

Figure 2.4 The drain current measurement as a function of the gate voltage at a 0.5 meV source-drain voltage at 4.2K after illumination, (a) for a single-80nm-gate FET, (b) for a dual-80nm-gate LARTFET.

3. A set of FETs including a 'railway gate' device in which the carriers are confined in both lateral dimensions by 'ties' across the two gate electrodes (Fig. 2.5), but which is otherwise similar to the above dual gate device. The substrate was modified primarily by making the n+ cap layer very thin so recess was necessary for the gate structure. At room temperature the devices behave as normal MODFETs as expected; the Ids/Vgs curves showed a smooth turn-on. At 4.2K (and with no illumination) the railway gate device shows several distinct conductance fluctuations and the separation between the fluctuations becomes less as the gate becomes less negative (Fig 2.6). This is consistent with the decrease in barrier height decreasing the separation between quasi-bound states. It was also observed that a much larger drain voltage (50 mV) was needed to smooth out the transconductance fluctuations thus suggesting that the three-dimensionally confined electrons show more marked resonance effects [Kroemer]. One control sample, a single gate MODFET, showed no conductance fluctuations. A closer control device had a 'monorail' gate which was similar to the railway gate except that, having only one rail, there was no confinement along the transport direction (Fig. 2.7). The Ids/Vgs curve for this device showed no conductance fluctuations where they occurred in the railway gate device although there are two weak fluctuations at large values of drain current.

In summary the low temperature conductance fluctuations seen in both the railway gate device and in the dual gate device are evidence of resonant tunneling effects in the transport of electrons through a lateral double barrier. The extra lateral confinement of the railway gate device appears to give rise to stronger resonance effects. When recently illuminated even single gate devices show conductance fluctuations and we believe such fluctuations arise from trap states.

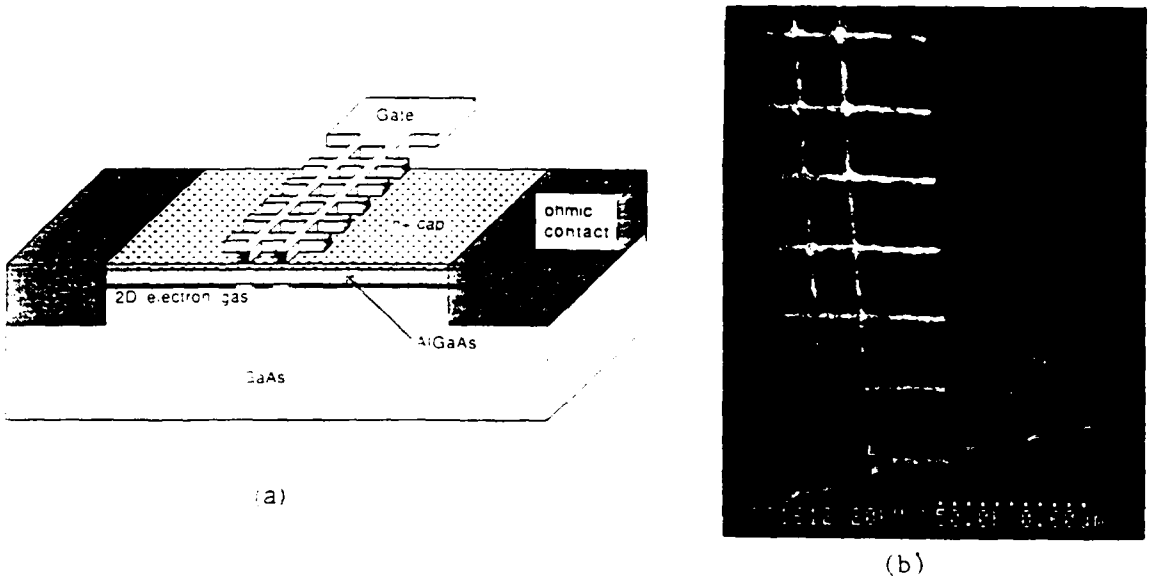

Figure 2.5 (a) Schematic of a railway gate lateral resonant tunneling field effect transistor, (b) scanning electron micrograph of the gate electrode. The width of the ties and rails is 50nm, the spacings between the ties and beteween the two rails are 230 nm and 150 nm, respectively. The ties are 750nm long.

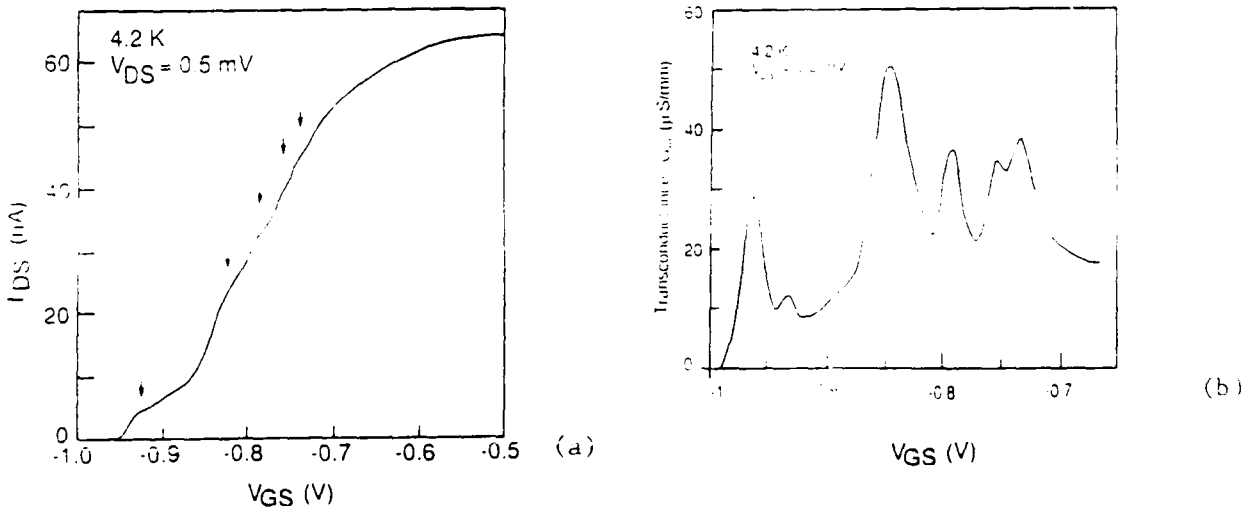

Figure 2.6 The drain current vs. the gate voltage and (b) the transconductance vs. gate voltage with a drain bias of 0.5mV at 4.2K for the railway gate lateral resonant tunneling field effect transistor. The arrows indicate the approximate location of the conductance oscillations.

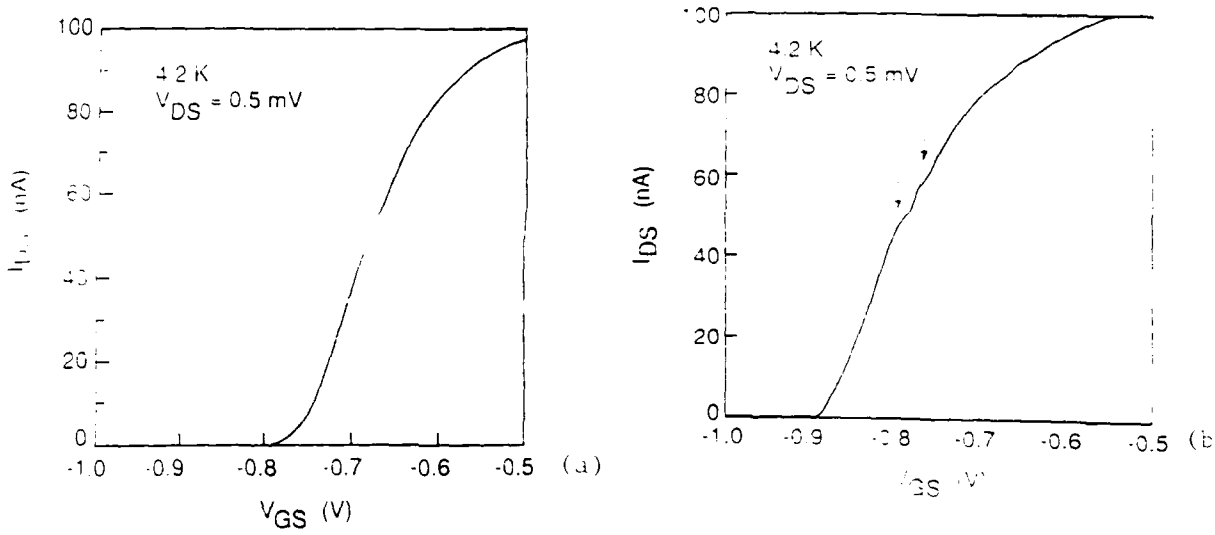

Figure 2.7 (a) The drain current vs. gate voltage with drain bias of 0.5mV at 4.2K for a solid gate controld evice (Lg = 0.9μm). No conductance oscillations are present. (b) Equivalent curve for the monorail device.

Ultra-small Devices Employing High T_c Superconductors

During the last part of the reporting period the research plans for superconducting devices were reviewed and some revision made as a result of progress in this field since the proposal was initially submitted. The main thrust is still to investigate the physics and device applications of high T_c superconductors fashioned with ultra-small lateral dimensions. It appears that the dimensions required for generating weak links are considerably finer than those used for the lateral resonant tunneling research; although some effects might be seen for features in the range 20nm to 50 nm (the finest that we have generated in the resonant tunneling project) it is desirable to generate lateral features less than the coherence length of these materials. Values of coherence length have been reported as high as 16 nm [Suzuki] but most reported values are below 5 nm. Two complementary approaches to achieving this resolution are being pursued. One is to employ brighter beams and higher resolution patterning processes [Mochel] and the the other is to improve the control of the process by monitoring the electrical characteristics of the workpiece during the patterning process. This second approach involves the use of a cooling stage either in the pattern generator itself or in the unit used for subsequent pattern transfer. Funds for the cooling stage are being sought from the Center for Materials Research. The work will be conducted in collaboration with members of the Ginzton Laboratory (Geballe, Beasley, Kapitulnik groups) who will provide the films and provide assistance in testing.

JSEP SUPPORTED PUBLICATIONS

1. D. R. Allee, J. D. Pehoushek and R. F. W. Pease, "Novel Monte Carlo simulation of space-charge-induced energy broadening laser irradiated cathodes," *J. Vac. Sci. Technol.*, **B6**, (6), 1989, Nov/Dec 1988.
2. S. Y. Chou, D. R. Allee, R. F. W. Pease and J. S. Harris, Jr., "Observation of electron resonant tunneling in a lateral dual-gate resonant tunneling field-effect transistor," *Appl. Phys. Lett.*, **55**, (2) 176, 1989).

JSEP SUPPORTED PRESENTATIONS

D. R. Allee, S. Y. Chou, J. S. Harris, Jr. and R. F. W. Pease, "Engineering lateral quantum interference devices using electron b;eam lithography and molecular beam epitaxy," presented at 1989 International Symposium on Electron, Ion and Photon Beam Technology, May 1989.

JSEP SUPPORTED DISSERTATION

D. R. Allee, "Nanometer Scale Device Engineering," Ph.D. dissertation, Stanford Electronics Laboratory, Stanford, CA, August 1989.

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Unit: 3

TITLE: Reactive Ion Profiling of Heterostructures

PRINCIPAL INVESTIGATOR: C. R. Helms

GRADUATE STUDENTS: Margaret Kniffin, Gregory Scott and Timothy Beerling

Scientific Objectives:

The objective of this work is to determine the surface chemistry associated with the interaction of reactive ions with GaAs and other III-V surfaces. Scientifically, this work represents an important new direction in studies of the interaction of neutral, stable molecules with surfaces. From a technological point of view, it will provide key information so that mechanisms of plasma and reactive ion processing of GaAs surfaces can be better understood. Our study will concentrate on the interaction of halogen containing molecular ions with GaAs surfaces. In-situ electron spectroscopy and mass spectroscopy techniques developed for similar studies of SiO_2 and Si [Thomson, 85], [Thomson, 86], will be employed in this investiga-tion. With this in mind, our specific objectives are:

1. To determine the relative importance of physical sputtering versus chemical reactions in GaAs reactive ion etching.

2. To determine the chemical nature of residues present during and after reaction ion bombardment.

3. Develop atomistic theoretical models to describe the combined effects of physical sputtering and chemical reactions during GaAs reactive ion bombardment.

Summary of Research:

In addition to the work proposed in this new contract, we have been continuing work begun on the previous program on metal-GaAs interfaces (the thesis work of Margaret Kniffin). This will be reported on first.

In our new work, the utility of halogens in conjunction with inert gas ions for in-situ reactive profiling of semiconductor structures has been assessed, initially using Si/SiO_2 interfaces as a test case [Scott]. In addition, since the program began, new results have

appeared indicating the utility of low temperature deposition and etching in downstream plasma reactors (in both RF and ECR microwave configurations). With this in mind we are beginning construction of a UHV compatible downstream plasma source which will initially be used to investigate cleaning and etching of III-V surfaces and Device Structures.

Schottky Barrier Properties of Gallium Intermetallic Alloy Contacts to GaAs

M. L. Kniffin and C. R. Helms

In the past year we established a technique by which to controllably and reproducibly fabricate a range of metal gallide thin films. Using this technique, metal gallide Schottky diodes on n-type gallium arsenide were fabricated and subjected to a variety of annealing cycles. Changes in both the interfacial chemistry and Schottky barrier properties were monitored as a function of annealing temperature. Correlations between the two were made and examined within the framework of existing models of Schottky barrier behavior.

To ascertain that homogeneous films of known composition could indeed be fabricated, films were evaporated onto silicon substrates from a range of initial Ag-Ga and Mn-Ga melt compositions. The resulting thin films were then characterized using electron microprobe analysis (EMP), X-ray diffraction analysis (XRD) and Auger sputter profiling (ASP) techniques. Figure 3.1 shows the EMP results for silver-gallium thin films. The solid line corresponds to the film composition predicted on the basis of thermodynamic data [Kubaschweski]. The points corresponds to actual measurements from as-deposited thin films. Similar results were found for the Mn-Ga binary system.

The films were analyzed for compositional and phase uniformity, using a combination of Auger depth profiling and x-ray diffraction. For compositions exceeding 70 percent Ag, the films were compositionally uniform and contained the phases predicted from the Ag-Ga equilibrium binary phase diagram. For more gallium-rich compositions, the films were non-homogenous and contained large amounts of liquid gallium. Compositionally uniform Mn-Ga films were also obtained for compositions ranging from 20 to 50 atomic percent manganese. Phase identification was not possible, however, as the grain size was extremely small.

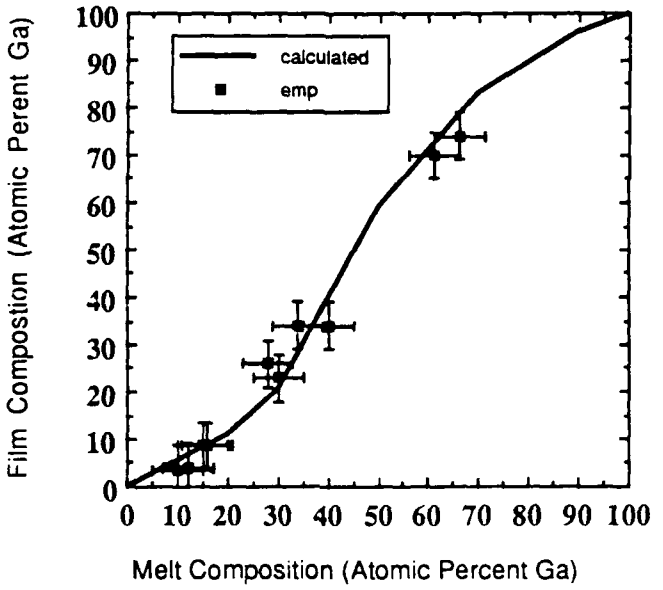

Figure 3.1 Silver-gallium alloy film composition as a function of alloy source composition. Solid line shows values calculated from thermodynamic data. Points are are actual films measured by an electron microprobe.

Using the technique described above, thin film Schottky diodes were deposited on n-type ($5x10^{16}$ to 10^{17} cm^{-3} silicon) GaAs. The diodes were then annealed in flowing hydrogen, at temperatures ranging from 170 to 600°C, for 15 minutes. Changes in Schottky barrier height were monitored by a combination of photoresponse, current-voltage and capacitance-voltage measurements. Interdiffusion and interfacial reactions were studied primarily with Auger sputter profiling techniques.

The effect of annealing on the Schottky barrier heights for Mn and Mn:Ga alloys is illustrated in Fig. 3.2. The as-deposited barrier heights for all of these interfaces are low (0.65 to 0.72 eV), but consistent with the range of values previously reported for low work function or low electronegativity metals on GaAs. After annealing, only the barrier height for the most gallium rich films (80 percent Ga) remained unchanged. These films were electrically stable up to about 450°C, the melting point of the thin film. Films richer in manganese behaved similarly to elemental manganese, with a large increase in the barrier height occurring at roughly 250°C.

An Auger depth profiles of the most Ga-rich film contain no evidence of interfacial reaction up to 450°C, close to the melting point of MnGa4. For the films higher in manganese content, some interfacial reaction similar to that of elemental Mn was detected, indicating these films are not thermodynamically stable with respect to GaAs. The nature of this interfacial reaction is clearly evident in the Mn-GaAs Auger depth profiles. At temperatures only slightly above those required to induce a large change in the Schottky barrier height, the formation of a distinct layer rich in Mn and As is visible. Similar chemistry can be deduced for the Mn rich alloy films. Increases in Schottky barrier height, on the order of 100 meV, upon formation of a metal-arsenide at the interface have been observed in other metal GaAs systems and explained by a variety of mechanisms [Kim], [Kniffin], [Spicer].

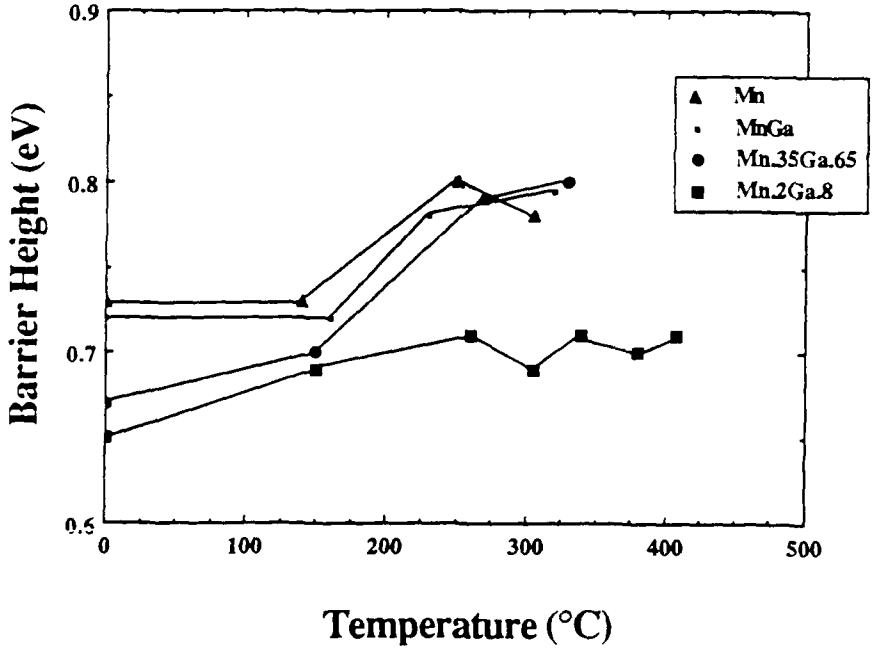

Figure 3.2 The effect of annealing on the Schottky barrier height of Mn and Mn-gallide contacts to n-type GaAs. Points were determined from capacitance-voltage and current-voltage measurements.

Panish established phase equilibria in the Ag-Ga-As system in the late 1960s [Panish]. On the basis of this work one would expect all of the silver-gallium alloy films to be unreactive with respect to GaAs. Au, although it's phase diagram is similar, does in fact react with GaAs. The explanation of this phenomenon is the selective loss of arsenic into the vapor phase [Pugh]. A rough thermodynamic calculation, similar to the calculations made for Au on GaAs [Predel], [Pugh], shows that while the driving force for this is favorable in the Au-Ga-As system it is not favorable in the Ag-Ga-As system. One would therefore expect all the Ag-Ga alloy films to be chemically stable with respect to the GaAs substrate.

The effects of annealing on the barrier heights of Ag, Ag doped with Ga and γ-AgGa (the most silver rich intermetallic) are illustrated in Fig. 3.3. Ag and g-AgGa exhibited reasonably stable electrical characteristics. The silver films tended to ball up at elevated temperatures, thus could only be studied to about 350°C. γ-AgGa films, exhibited much better adhesion and were stable up to their melting point (about 500°C). It should be noted that measured values for the γ-AgGa contact did decrease slightly upon annealing to yield an anomalously low barrier height (0.59 to 0.64 eV).

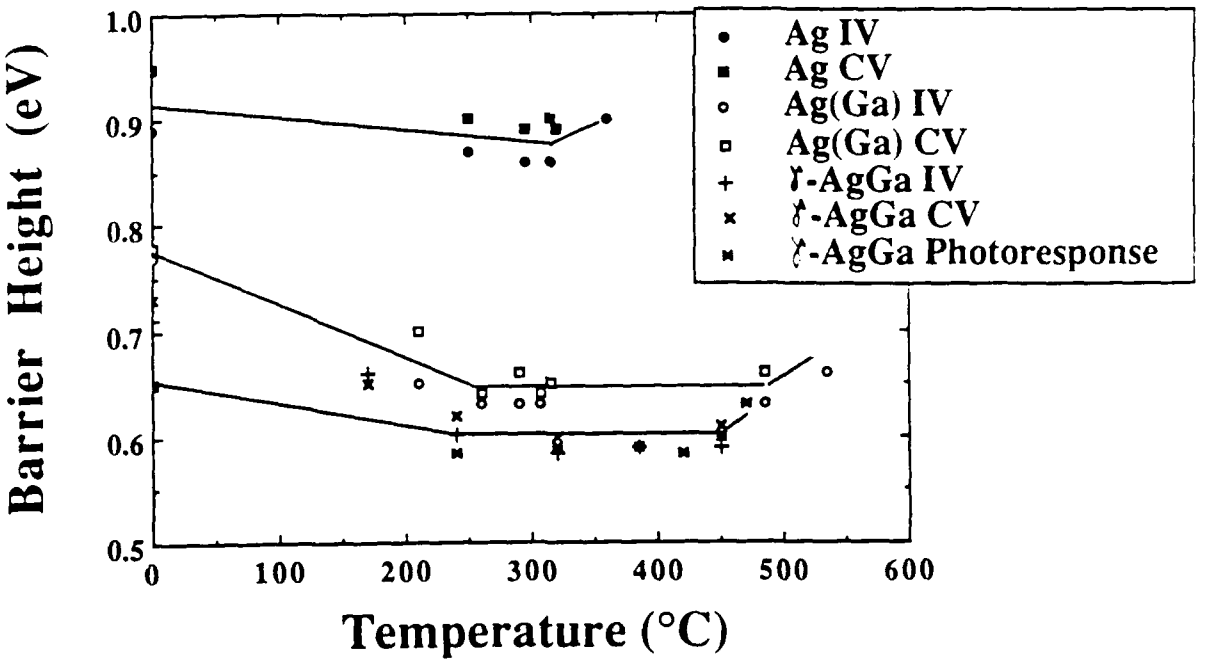

Figure 3.3. The effect of annealing on the Schottky barrier height of Ag and Ag-Ga alloy contacts to n-type GaAs. Points were determined from capacitance-voltage and current-voltage measurements.

The Ag doped with gallium (3.5 percent) behaved in an unexpected manner. The barrier heights for these contacts were already somewhat lower than the barrier heights observed for pure Ag on GaAs. Upon annealing, the barrier height decreased even further, to values closer to that of γ-AgGa. At temperatures above 550°C, these diodes became non-rectifying (although it is not clear if this is a leakage effect or not).

No large scale interactions between the Ag and Ag-Ga alloy films were detected in the Auger depth profiles. Although the simplest explanation for the electrical behavior of the contacts containing Ag doped with gallium would be to assume the existence (or formation) of regions of γ-AgGa at the interface, XRD, Auger and preliminary TEM results have given no evidence of this. At this point in time it would appear that the electrical properties must be attributed to something other than the formation of a new, lower work function phase at the interface. Further work in this area is currently being undertaken.

In general the barrier heights of the stable metal-gallide contacts were quite low. Similar barrier heights have been reported for other metal-gallide contacts to n-type GaAs. The low barrier heights observed for metal-gallide contacts to n-type GaAs are surprising in light of recent reports of extremely high barriers to GaAs for Ga and Ga-rich contact systems [McClean], [Svensson]. It is also somewhat inconsistent with the predictions of the AUDM [Spicer]. Further work in this area is in progress and could lead to some interesting insight as to the mechanism(s) controlling Schotkky barrier formation in gallium arsenide.

Reactive Ion Interactions

In our previous work on Si, reactive ions such as CF_3^+ or SF_5^+ were employed for reactive sputtering of Si_2 and Si. These species could be produced from inert gasses CF_4 and SF_6 but led to carbon and sulfur poisoning of surfaces. This led us to assess another approach using the halogen such as F_2, Cl_2, etc.) directly with a separate inert ion beam. Initial results in tests on Si and SiO_2 surfaces [Scott] show that much better results are obtained than with CF_3^+ or SF_5^+ and of equal importance the F_2 can be handled in our current UHV systems. More details are available in [Scott].

Downstream Plasma Processing

Recent work using downstream plasma processing for low temperature depositions have resulted in operating MIS devices on GaAs [Fountain] as well as high quality Si MOS devices [Richard] using low temperature grown oxides. These existing results have led us to change direction for the future in this program to construct such a reactor on an existing UHV surface analysis system. In our first experiments with this approach the utility of such a reactor, operating with either hydrogen or oxygen, for surface cleaning will be assessed. Other plans include the investigation of Si-Ge deposition and SiO_2 deposition on

both Si and GaAs at low temperatures for surface passivation.

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JSEP Supported Publications

1. K. B. Kim, M. Kniffin, R. Sinclair, C. R. Helms, "Interfacial Reactions in the Ti/GaAs System", *J. Vac. Sci. Tech.* **A6**, 1473 (1988).
2. G. Scott, K. Ninomiya, C. R. Helms, I. Lindau, "Auger Analysis of Si Sputtered with Ar+ Ions in an F_2 Ambient", *Surface Science*, in press.

JSEP Supported Presentations

M. Kniffin, C. R. Helms, "Schotky Barrier Properties of Gallium Intermetallic Alloy Contacts to GaAs", 1989 Electronic Materials Conference, Boston.

Unit : 4

TITLE: GaAs on Si Integrated Circuits

PRINCIPAL INVESTIGATOR: B. A. Wooley

GRADUATE STUDENT: G. Nasserbakht

Scientific Objectives:

The objective of this research is to investigate means by which newly emerging compound semiconductor technology, such as heteroepitaxial GaAs on Si, can be exploited at the circuit and system level. The emphasis of the program is on application of GaAs/Si technology to optoelectronic circuits for broadband communication circuits.

Summary of Research:

Advances in current VLSI technology have made it possible to process data and signals at increasingly higher rates. This enhanced processing capability has in turn put increasing demands on data communication channels. In a fiber optic communications system, stringent bandwidth and sensitivity requirements are placed on the receiver electronics. These requirements are especially significant at the front-end of the receiver, where the optical information is converted to an electronic format and subsequently amplified by the preamplifier circuitry. The parasitic elements associated with the interconnection of the photodetector and the preamplifier usually limit the overall system performance. Monolithic integration of these components would overcome this limitation by decreasing the parasitic interconnection capacitance. The main obstacle to achieving such integration is the necessary transition between two different semiconductor technologies that usually occurs within the optical/electronic interface. Compound semiconductors, due to their optoelectronic properties, are the materials of choice for photodetectors, while in most cases silicon is generally the preferred material for the front-end receiver since the receiver electronics are then readily compatible with the subsequent VLSI circuitry often used for signal and data processing. Successful epitaxial growth of compound semiconductor materials such as GaAs films on Si substrates, has made it possible to merge these technologies in order to achieve significant improvements in system performance.

One focus of this research is the design of a fiber optic receiver front-end consisting of a GaAs photodetector and a Si preamplifier. The circuit schematic of this receiver is shown in Fig. 4.1. The photodetector is an interdigitated MSM (Metal-Semiconductor-Metal)

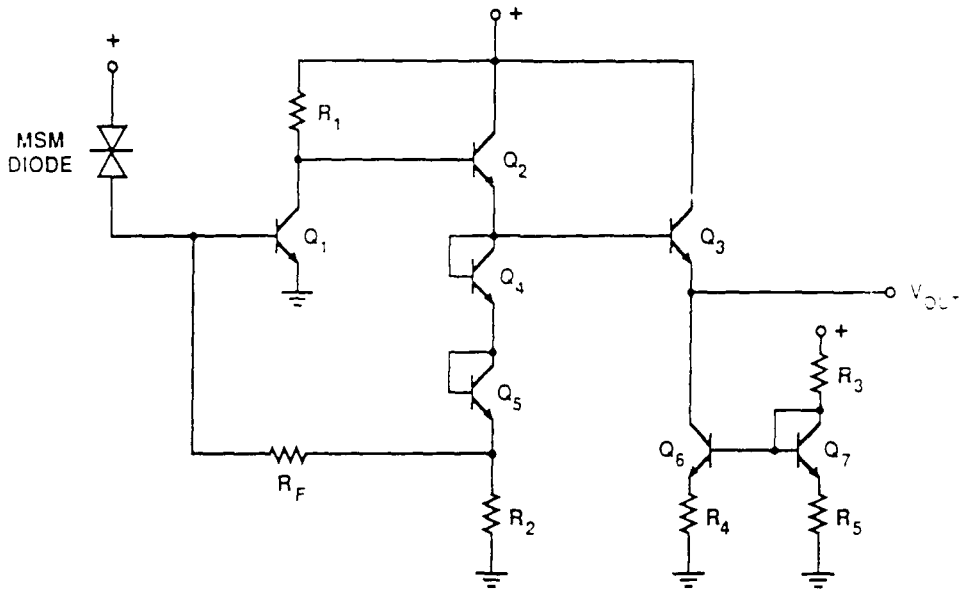

Figure 4.1.Circuit schematic of the preamplifier and the photodiode.

Schottky-barrier photodiode. It consists of multiple 3μm-wide stripe electrodes and has an area of 100μm square. The preamplifier is a transimpedance design using a shunt-series feedback configuration. This circuit was integrated at Hewlett-Packard in a Si VLSI bipolar technology with a polysilicon-emitter structure.

The transimpedance gain of the preamplifier in Fig. 4.1 is determined by the value of the feedback resistor R_F. The bandwidth of the preamplifier is inversely proportional to the total capacitance at the input, including the input capacitance of the preamplifier, the photodiode capacitance, and any parasitic capacitance associated with the input node. The input noise current density decreases with decreasing total input capacitance. Monolithic integration of the photodiode and the preamplifier thus results in improved bandwidth and noise performance for the receiver by decreasing the parasitic interconnection capacitance at the input. The receiver has been designed to operate at a bandwidth of about 1GHz and a transimpedance of 5KΩ. Measurements on photodiodes fabricated on Si substrates without the receiver circuitry show a maximum internal responsivity of about 0.2A/W, with a pulse response of less than 100ps FWHM. The S_{21} gain of an experimental preamplifier, without the photodetector, was measured using a network analyzer. The results, an S_{21} gain of 20db with a bandwidth of about 400MHz, were in agreement with the simulated values.

To integrate the photodetector and preamplifier monolithically, the Si circuits were removed from the Si fabrication line prior to metallization. Using an anisotropic KOH etch, recessed Si trenches were formed in which epitaxial GaAs was grown using an MBE process. GaAs photodiodes were subsequently fabricated in these regions and the entire circuit was then metallized. Due to the short supply of available processed Si wafers, each wafer was divided into quarters and each piece was further processed separately. This resulted in some unavoidable processing difficulties, since all back-end processing steps, especially metallization, were optimized for full wafers. Our first processing run resulted in functional circuits. These circuits, however, operated at very low speed due to unintentional contamination of the contact regions that resulted in very high contact resistances. In two additional runs, the process was further optimized and the metal dry etch process was re-designed for use with partial wafers. We are currently starting another fabrication run of the receiver. Upon completion of this run, we should be able to test the performance of the receiver front-end at high speed.

Since CMOS is clearly the technology of choice for current VLSI systems, design of the front-end preamplifier in CMOS would improve the level of integration for the complete receiver, including the data recovery and signal processing circuits that follow the preamplifier. As part of this research, we have started to investigate the design and integration of a Si CMOS preamplifier with a GaAs MSM photodiode. In order to determine the effects of GaAs growth and further processing steps on the MOS transistor characteristics, a test mask has been designed and is currently being fabricated at Intel Corporation. This test mask contains N and P channel transistors of various sizes at various distances from the grown epitaxial GaAs region. The design of a CMOS preamplifier is currently underway. We are studying the tradeoffs involved in using various designs for the input stage, such as the common-gate or common-source structure. The common-gate input stage can result in wide bandwidth operation, but has degraded noise performance compared to the common-source stage. Various kinds of feedback configurations are also being studied. The objective of this research is not only to demonstrate the monolithic integration of GaAs and Si MOS devices and circuits but also to design a high bandwidth GaAs/CMOS front-end for an optical receiver that would be useful in applications such as local area networks and optical system interconnections.

JSEP Supported Publications

G. N. Nasserbakht, J. W. Adkisson, T. I. Kamins, B. A. Wooley and J. S. Harris, Jr., "A Monolithically Integrated Fiber-Optic Front-End Receiver in GaAs on Si Technology", *Symp. VLSI Circuits Dig. Tech. Papers*, p. 83, May 1989.

Unit: 5

TITLE: THE ELECTRONIC STRUCTURE OF HIGH TEMPERATURE SUPERCONDUCTORS

SENIOR PRINCIPAL INVESTIGATORS: I. Lindau and W.E. Spicer

POST-DOCTORAL FELLOWS: Z.-X. Shen and P. A. P. Lindberg

GRADUATE STUDENTS: D. S. Dessau and B. O. Wells

Scientific Objectives:

The recently discovered copper-oxide based high temperature superconductors are of great interest both from a scientific and a technological viewpoint. The objective of this work is two-fold: first, to provide a better understanding of the electronic structure of these and related materials, ultimately aimed at gaining an understanding of the mechanism of the high temperature superconductivity, and secondly, to detail the behavior of interfaces of the high temperature superconductors with other technologically important materials.

Summary of Research:

We have used a variety of surface-sensitive spectroscopic techniques in our studies of the high temperature superconductors. These are X-ray Photoemission Spectroscopy (XPS), Ultraviolet Photoemission Spectroscopy (UPS), and Low Energy Electron Diffraction (LEED). The photoemission spectroscopy was performed in both angle-integrated and angle-resolved modes.

A. Intrinsic properties of the high temperature superconductor $Bi_2Sr_2CaCu_2O_8$

Most of our work during the past year was performed on this family of high temperature superconductor, primarily because the highest quality single crystals of these materials were available, and their inertness in ultrahigh vacuum conditions. LEED was used to confirm the single crystallinity of the in situ cleaved crystals of $Bi_2Sr_2CaCu_2O_8$. Sharp diffraction spots indicative of long range periodicity were observed. The observed LEED pattern showed that the crystals preferentially cleave parallel to the a-b plane. In addition, a superstructure was found to have a periodicity about 5 times as long as the cell

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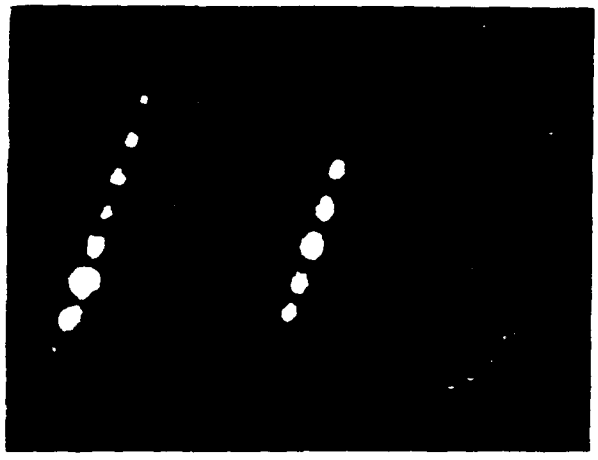

Figure 5.1 LEED pattern of a freshly cleaved $Bi_2Sr_2CaCu_2O_{8+d}$ single crystal using 40 eV electrons

dimensions of the a and b axes (Fig. 5.1), in agreement with bulk sensitive measurements such as x-ray diffraction.

XPS studies revealed single component oxygen 1s emission, suggestive of contamination-free surfaces, and a Cu2p satellite to main line intensity ratio of 0.3-0.4. The presence of the strong Cu2p satellite is taken as evidence that that the $Bi_2Sr_2CaCu_2O_8$ material contains unfilled 3d electronic states. In addition, energy-loss spectroscopy of the photoelectrons of different elements of the crystal was performed. Utilizing the fact that photoelectrons of different elements are excited at different locations in the unit cell, we were able to identify the energy-loss features as due to valence plasmon excitations and one-electron excitations. Our results were consistent with other, bulk sensitive measurements, implying that the electronic structure of the near surface region, which photoemission probes, is representative of the bulk electronic structure.

PS studies revealed an appreciable density of states at the Fermi level, showing the metallic nature of the material. The related compound $Bi_2Sr_2CuO_6$, which has a lower superconducting transition temperature than $Bi_2Sr_2CaCu_2O_8$, showed a lower density of states at the Fermi level, consistent with its lower T_c. As an explanation, we suggested the coexistence of bandlike p states of Bi-O origin and correlated Cu 3d-O 2p bands.

Our angle-resolved studies showed essentially dispersionless character of the valence band states as a function of the wave vector component parallel to the c-axis, while clear dispersion of the order of 0.3-0.4 eV was observed as a function of the wave vector component parallel to the a-b plane. This result, which is consistent with the macroscopic properties of the $Bi_2Sr_2CaCu_2O_8$ material, confirms that virtually all the hybridization among the Cu3d and O2p states is confined to the two dimensional layers. In addition, we utilized the polarized nature of the synchrotron radiation to probe the symmetries of the various valence band features. This facilitates comparison of experimental with theoretical features.

B. Studies of Interfaces between metals and $Bi_2Sr_2CaCu_2O_8$

Our studies of metal overlayers on superconductors have centered on understanding the chemistry of the metal-superconductor interface. We focus on four metals: aluminum, rubidium, silver, and gold. A metal overlayer experiment is performed in several steps. First a clean surface is prepared by cleaving a clean surface in vacuum. The clean surface is studied by photoemission as a reference. Then a small overlayer of metal (about 1 Å) is evaporated onto the surface and again studied by photoemission, and the process is repeated to build up an overlayer.

Photoemission has proven to be a powerful technique for studying surface chemical reactions and chemical states. The chemical information is revealed by studying the shape and binding energy of the atomic core levels. For example the Cu2p level has two components that are split in energy by the spin-orbit interaction. For metallic copper, only two, fairly sharp features are seen in the Cu2p spectrum. However, for doubly ionized Cu, such as in CuO, the features broaden and each spin orbit split component has a higher binding energy satellite.

Al was deposited as an example of a typical metal. After Al deposition, the Bi peak shifted 2 eV to lower binding energy. Similarly, by the time 2 Å of Al were deposited, the Cu2p satellites had disappeared. Clearly both the Bi and Cu layers had been reduced. The surface appears to be heavily reacted and contains several oxides rather than resembling the superconductor. This heavily reactive behavior is typical of most metals including Ti,Cr,Bi and even a noble metal, Cu.

Rb is a reactive metal that does not fit the usual pattern. It is an alkali metal and in most situations is extremely reactive. However, when Rb is deposited on the $Bi_2Sr_2CaCu_2O_8$ surface only a minor reaction occurs. The $Bi4f_{7/2}$ peak shifts about 0.5 eV to higher binding energy. However the Cu2p peaks show no sign of a reaction. Rb is a very large

atom that does not tend to diffuse well in most materials. Apparently the Rb remains on the surface of the superconductor and reacts only with the surface layer.

Ag and Au are both noble metals and are the only materials that we have studied that do not show a strong reaction. Ag does show some movement of the core level peaks and the Cu2p satellite intensity ratio does decrease with greater Ag coverage. Apparently there is a small amount of Ag oxide formation and a reduction of the Bi and Cu planes. Also the cation core levels show a slower than expected attenuation with increasing Ag coverage leading us to suspect some diffusion of Ag into the superconductor substrate. Au however seems to cover the superconductor surface without any detectable chemical reaction and does not show signs of interdiffusion with the superconductor.

The above information about the chemical nature of the metal/superconductor interface suggests fruitful directions for many important basic studies. First of all Au and Ag seem to be the most likely candidates for low resistance contacts to $Bi_2Sr_2CaCu_2O_8$. Indeed several studies have shown that evaporated Au or Ag make the best contacts. Alkali metals may be a very interesting tool for studying the various layers of $Bi_2Sr_2CaCu_2O_8$ independently since it can disrupt the surface Bi-O layer but not the important Cu-O layer. Finally, Au appears to be the best overlayer metal to study the proximity effect - where a normal metal in close proximity to a superconductor will become superconducting itself. To observe this effect we must have a smooth conducting surface in extremely close electrical contact with a superconducting surface. It has not yet been demonstrated whether or not the proximity effect exists for the high T_c superconductors. The effect is important from both technological and theoretical perspectives. Technologically, it is much easier to work with an inert Au surface than the $Bi_2Sr_2CaCu_2O_8$ surface and may be critical if a superconducting surface is needed. We are presently conducting an extensive search for the proximity effect with inconclusive results up to this time.

JSEP-SUPPORTED PUBLICATIONS:

1. Z.-X. Shen, P. A. P. Lindberg, B. O. Wells, D. B. Mitzi, I. Lindau, W. E. Spicer and A. Kapitulnik, "Valence Band and Core Level Photoemission Study of Single-Crystal $Bi_2Sr_2CaCu_2O_8$ Superconductors", *Phys. Rev. B* **38**, 11820 (1988).
2. Z.-X. Shen, P. A. P. Lindberg, D. S. Dessau, I. Lindau, D. B. Mitzi, I. Bozovic and A. Kapitulnik, "Photoelectron energy-loss study of the $Bi_2Sr_2CaCu_2O_8$ superconductor", *Phys. Rev. B* **39**, 4295 (1988).
3. Z.-X. Shen, P. A. P. Lindberg, W. E. Spicer, I. Lindau and J. W. Allen (Invited paper), "Photoemission Study of High Temperature Superconductors", {Invited paper for AVS, 1988, Atlanta} to be published in the *AIP/AVS Conference Proceedings*,

182, (1989).

4. Z.-X. Shen, P. A. P. Lindberg, B. O. Wells, I. Lindau, W. E. Spicer, P. Soukiassian, D. B. Mitzi, C. B. Eom, A. Kapitulnik and T. H. Geballe, "Surface and Electronic Structure of Bi-Ca-Sr-Cu-O Superconductors Studied Using LEED, UPS and XPS", to be published in the *AIP/AVS Conference Proceedings,* 182, (1989).
5. P. A. P. Lindberg, Z.-X. Shen, I. Lindau, W. E. Spicer, C. B. Eom and T. H. Geballe, "Photoemission study of the surface electronic structure of Bi-Ca-Sr-Cu-O superconductors modified by Ne-sputtering, Ag-deposition and heat treatment", *Appl. Phys. Lett.* **53**, 529 (1988).
6. P.A.P. Lindberg, P. Soukiassian, Z.-X. Shen, C. B. Eom, I. Lindau, W. E. Spicer, T. H. Geballe, "Electronic structure of ceramics and thin film samples of high-Tc $Bi_2Sr_2CaCu_2O_8$ superconductors: effects of Ar^+-sputtering, O2-exposure and Rb-deposition", *Appl. Phys. Lett.*, **53**, 1970 (1988).
7. P.A. P. Lindberg, Z.-X. Shen, B. O. Wells, D. Mitzi, I. Lindau, W. E. Spicer and A. Kapitulnik, "Surface strcture of $Bi_2Sr_2CaCu_2O_8$ high-temperature superconductor studied using low-energy electron diffraction", *Appl. Phys. Lett.* **53**, 2563 (1988).
8. B. O. Wells, P. A. P. Lindberg, Z.-X. Shen, D. S. Dessau, I. Lindau, W. E. Spicer, D. B. Mitzi and A. Kapitulnik, "Aluminum and Gold Deposition on Cleaved Single Crystals of $Bi_2Sr_2CaCu_2O_8$ Superconductors", to be published in the *AIP/AVS Conference Proceedings* 182, 1989.
9. P. A. P. Lindberg, Z.-X. Shen, B. O. Wells, D. S. Dessau, D. R. Mitzi, I. Lindau, W. E. Spicer and A. Kapitulnik, "Reaction of Rb and oxygen overlayers with single-crystalline $Bi_2Sr_2CaCu_2O_8$ superconduc-tors" *Phys. Rev. B* **39**, 2890 (1989).

Unit: 6

TITLE: Semiconductor Laser with Ultra-Low Threshold Current

PRINCIPAL INVESTIGATOR: S. S. Wong

GRADUATE STUDENT: To be determined

Scientific Objectives:

The objective of this work is to study the interplay between geometry and physics in a semiconductor laser in order to achieve ultra-low threshold current. This project was initiated in July of 1989, and hence only a limited amount of result has been obtained during this reporting period.

Summary of Research:

1. Defect Induced Intermixing Of Quantum Well

Semiconductor lasers with quantum wells, which provide one-dimensional confinement of carriers have proven to be extremely efficient devices. Theoretical calculations have revealed that two-dimensional confinement using a quantum wire structure will further reduce threshold current and improve efficiency. Attempts to create quantum wire structures include dry or wet etching, selective intermixing by ion implantation, and defect induced intermixing. Preliminary results on the latest technique are described.

A method to induce impurity-free vacancy diffusion is to apply a SiO_2 layer on the quantum well material. At high temperatures, the Ga atoms segregate into the SiO_2, thereby creating a very large number of site III vacancies. The vacancies diffuse into the bulk and cause intermixing of the Ga and Al atoms. The net effect is that some of the Ga atoms leave the QW and are replaced by Al atoms. This changes the band-gap of the QW and results in a blue shift in the photoluminescence spectra. Figure 6.1 shows the initial experimental result obtained. The sample was annealed by rapid thermal technique. By examining the intensity of the PL, it appears that no degradation of the material has occurred and the excitonic behavior remains very strong.

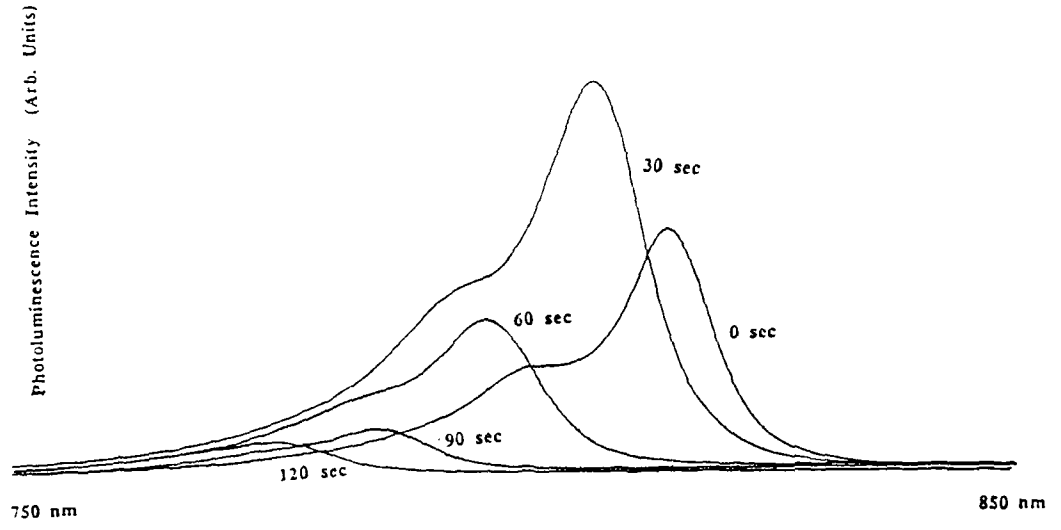

Figure 6.1. Room Temperature photoluminescence of SiO_2 capped single quantum well material. The sample was rapid thermal annealed at 850°C.

Unit: 7

TITLE: Device Physics and Technology of Silicon Based Heterostructures

PRINCIPAL INVESTIGATOR: J. D. Plummer

GRADUATE STUDENT: B. Biegel

Scientific Objectives:

The central objective of this research is to determine the potential for using silicon-based heterostructures in quantum electronic devices. These are a new genre of electronic devices whose basic operation is controlled by quantum effects such as charge carrier tunneling and interference. Our effort during this reporting period can be separated into two phases: 1) determination of the research project direction and goals, and 2) implementation of the first phase of this plan, the development and testing of a rudimentary computer simulator for quantum devices. Results of initial simulations and their implications are described below.

1. Research Direction

This research centers on a relatively new approach to an old goal in the electronics industry. The goal is to improve the speed of electronic devices (and hopefully the systems they compose) through scaling of the active region width of the devices. However, as the critical dimensions of conventional devices have decreased relentlessly, in some cases it is no longer possible to suppress, overwhelm, or even ignore, quantum effects. The new approach considered in this research is to actually employ quantum effects, such as tunneling and interference, in the operation of electronic devices. This approach allows the active region dimension of the device to be reduced into the quantum regime; typically 20 nm or less [Bate]. A quantum device also should allow the fundamental quantum efficiency limit to be approached much more closely.

Although a sufficiently narrow research topic is necessary in order to pursue it in depth, we also hoped that this research would provide a broader applicability to the growing field of quantum electronics. The solution to this in our case was to develop a general quantum device simulator, and then use this simulator in the analysis of SiGe-based heterostructure quantum devices. Thus, theoretical analysis and simulation would be used to optimize ideal devices first, and fabrication and testing would then build on these predictions in the context of real world nonidealities. The process is iterative, of course, since testing results

will be used to improve simulation models, and the simulation/testing process repeats.

For our simulation approach, we chose to build on a very basic quantum device simulator written previously by the graduate student involved in this research project. This simulator is based on a first principle quantum mechanical transport equation (analogous to the classical Boltzmann transport equation) that determines a function called the Wigner distribution of charge carriers (electrons or holes) and its evolution in the device. The Wigner function method allows one to see what is happening at every point in the device at all times, providing much more insight into the details of device operation, and thus more understanding of, and confidence in, the simulation results. The trade-off is, of course, the substantial computational effort required in using this physical simualtion approach. The unique instabilities of this numerical simulation method were first tamed by [Frensley].

The final issue to be addressed regarding the direction of research concerned the structures which would be investigated. The existing simulator was designed for the resonant tunneling diode (RTD), which is a layered structure with the center layer being a quantum well for charge carriers. Figure 7.1 shows the heterolayer structure and valence band of a p-type (hole) SiGe RTD. The RTD is the simplest device demonstrating all the relevant quantum phenomena (free propagation, interference, and tunneling). This structure has thus been considered as the prototype quantum device. As such, it has been widely studied empirically, analytically, and numerically as an n-type (electron) device in the GaAs material system. In fact, the Wigner function method has been used by Frensley on a GaAs RTD, so we decided to verify the accuracy of our simulator in the GaAs system first. Following this, we would perform an in-depth simulation analysis of p-type SiGe-based RTDs. The progress on these tasks is described below, and the plan for future goals is discussed in the final section.

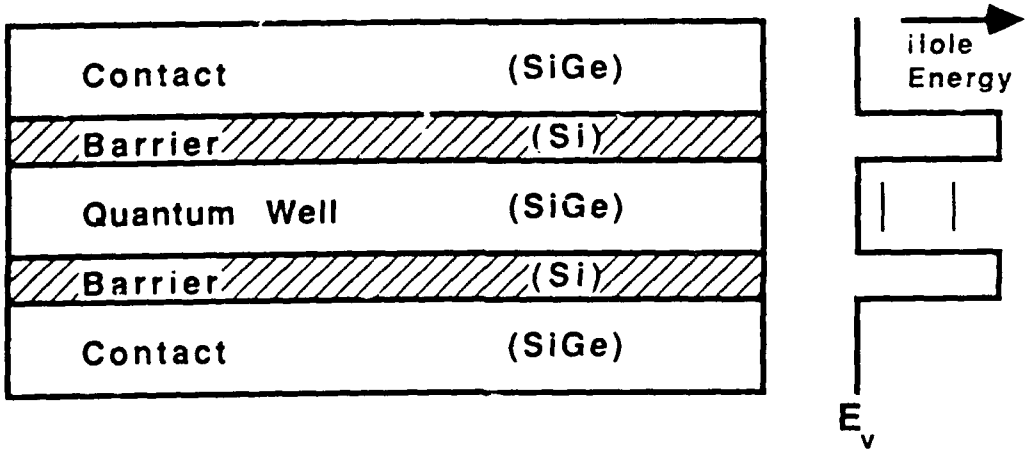

Figure 7.1 P-type SiGe RTD structure and valence band.

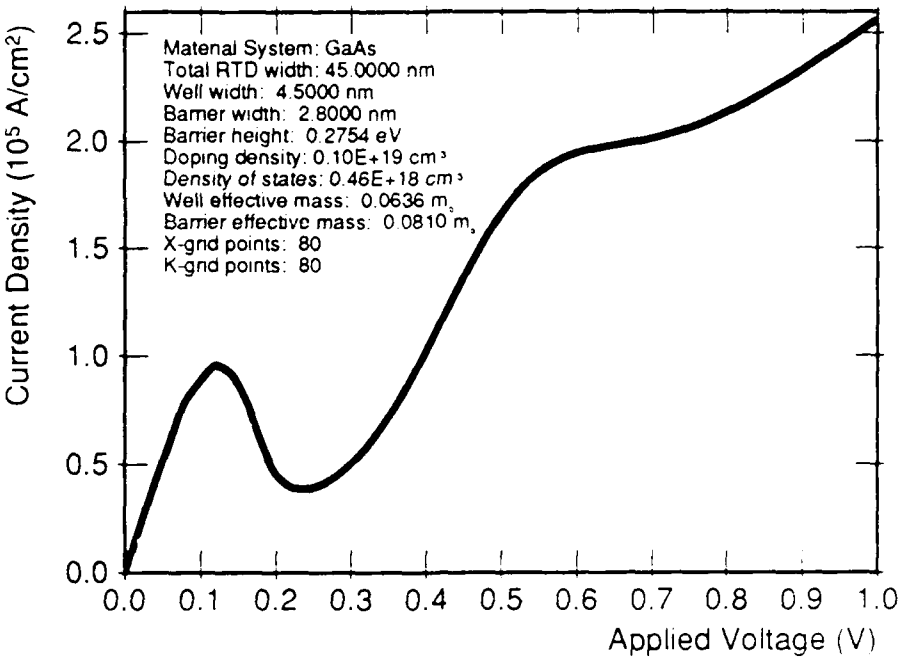

Figure 7.2 GaAs RTD I-V characteristic.

2. Quantum Simulator Testing

As stated previously, the simulation effort of this project builds on a very rudimentary simulation program, designed to model the steady-state operation of resonant tunneling diodes, which was already written. The first task accomplished during this reporting period was to verify the correct operation of this RTD simulator. To accomplish this we first simulated the I-V response of the exact GaAs RTD structure reported by Frensley. The resulting I-V characteristic (Fig. 7.2) was essentially identical to that of Frensley, which seemed to confirm correct operation of the simulator. However, initial simulations of SiGe RTDs produced unphysical results, such as negative power consumption.

After a few additional simulations, the crucial difference between the GaAs and SiGe structures was determined to be the differing effective masses of the materials. Using a narrower active region in our simulated device structure was found to remove this problem, and the expected I-V characteristic, including the negative differential restance (NDR) region observed empirically in RTDs, was then observed for SiGe-based structures (Fig. 7.3).

To verify the accuracy of our implementation of this simulation method, several fine-grid simulations were performed, with the result that both the standard-grid and the fine-grid (i.e., more accurate) simulations gave virtually identical I-V curves. To further verify the integrity of our simulator, the program was modified to allow the plotting of the Wigner function itself. The GaAs result was compared to that published by Frensley, and the two again appear to be identical. This verified that our implementation worked as it should.

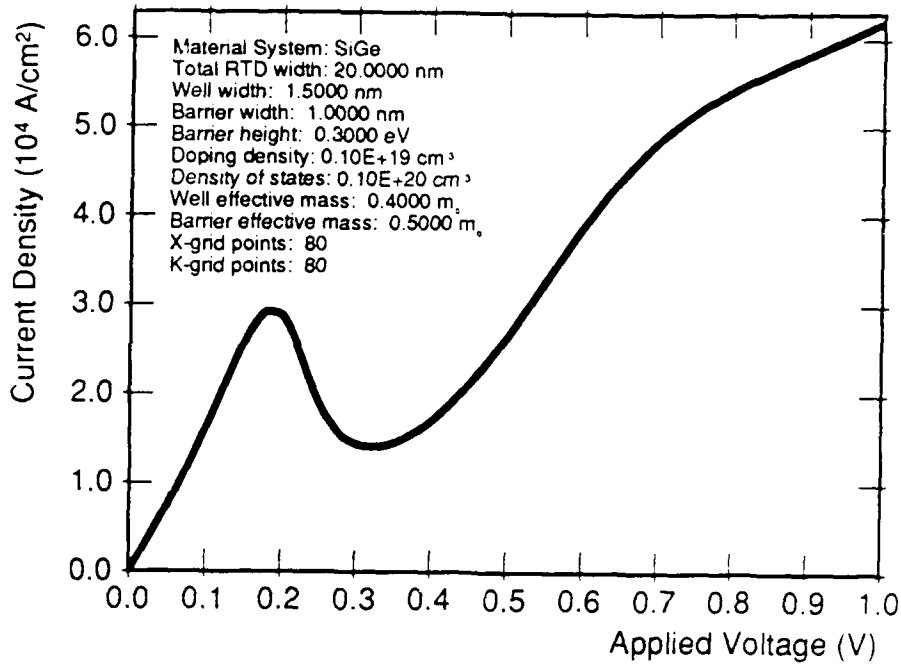

Figure 7.3 SiGe RTD I-V characteristic.

Having confirmed the integrity of our steady-state quantum device simulation program, further simulations were performed on SiGe-based structures. The Wigner distribution function for these devices, as for the GaAs RTDs, shows several quantum effects occurring, including quantum interference, exclusion from the well, and a negative probability of finding an electron in some barrier regions. The main difference between the SiGe and GaAs structures is that, due to the higher effective mass of holes in SiGe as compared to electrons in GaAs, the quantum wavelength is shorter in SiGe RTDs, so all quantum effects occur on a shorter scale (factor of 2 to 3) in this material. The shorter quantum wavelength thus requires a reduced barrier width in SiGe for useful current levels to be achieved. Further, it requires a reduced quantum well width, so that the quantized energy levels in the well are sufficiently separated for a high peak-to-valley current ratio (PVR), a principle figure of merit for an RTD in steady-state.

The process of optimizing the SiGe RTD structure for maximum PVR is ongoing. At present, simulations giving a PVR greater than 2 have been run, which is as good as those found for the GaAs test structure, although current levels are lower. The trade-offs, such as high current versus high PVR as determined by the barrier width, are still being evaluated as well. Modification of the simulation program to automate the creation of input data files and output plots has greatly accelerated these investigations. It also will aid in the determination of whether any remaining weaknesses (e.g., due to simplifying assumptions) exist in our implementation of the Wigner function simulation approach.

3. Future Directions

Several tasks currently underway should be resolved within the coming reporting period. 1) We will improve, if possible, the robustness of our simulation program so that it can deal accurately with any reasonable RTD structure. 2) We will complete the optimization, through steady-state simulation, of the SiGe RTD strucutre, and analyze any trade-offs that exist in this optimization. 3) Finally, an initial assessment (based on the steady-state RTD simulation results) of the prospects of using SiGe-based heterostructures in quantum devices will be made, especially in comparison with GaAs-based heterostructures.

Several important capabilities need to be added to our simulator before it can be used as a general quantum device simulator. First, the ability to model the transient response of the structure to changing applied biases will be incorporated, allowing us to assess the prospects of using silicon-based heterostructure devices to create faster electronic systems. Another important enhancement to be implemented is self-consistency between the electron distribution and the electrostatic potential profile of the device. Rather than drastically improving RTD simulation accuracy, however, the actual importance of implementing self-consistency is that the RTD simulator then becomes a general 1-D quantum device structure simulator simply by specifying the desired simulation structure. Also, pseudo three terminal devices could be simulated meaningfully by specifying the potential at a point internal to the device (as a third terminal would do in, say, a BJT). Finally, dissipative effects (due to charge carrier collisions) will be implemented in the program. These effects one of the major differences between GaAs and SiGe-based quantum devices.

Ultimately, it is desirable to have the capability to simulate 3-D quantum devices, rather than the present capability to handle only 1-D structures. This would allow true three (and more) terminal quantum structures to be simulated. The additional computational effort will obviously be extreme, as will be the reprogramming necessary to convert from a 1-D to a 3-D simulator. However, there is no equally capable alternative, and the information such a simulator could provide might finally allow us to see how three dimensional integration of quantum devices might be achieved and what the characteristics of a quantum integrated circuit might be.

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Unit: 8

TITLE: MOS Devices Based on the Ge_xSi_{1-x}/Si Material System

PRINCIPAL INVESTIGATOR: K. C. Saraswat

GRADUATE STUDENT: T. King

Scientific Objectives:

The long-term objective of this work is to investigate the potential use of epitaxial Ge_xSi_{1-x} layers in MOS devices. During the reporting period, the focus of this work has been on the formation of thin (less than 300 Angstroms thick) epitaxial layers of Ge_xSi_{1-x} on silicon by steam oxidation of Ge-implanted silicon which causes the germanium to be piled up into a thin layer at the silicon-dioxide/silicon interface.

While the advantages of fabricating heterojunction bipolar transistors in the Si/Ge_xSi_{1-x}/Si material system have been investigated and are well known, it is not yet clear whether the presence of a Ge_xSi_{1-x} layer would be advantageous in MOS devices. It is worth investigating the effects of an epitaxial, strained layer of Ge_xSi_{1-x} in the channel region of a MOS device; this might lead to important implications for heterostructure BiCMOS technology. Although the energy band structure of the Ge_xSi_{1-x}/Si system is not necessarily favorable for use in MOS devices, the presence of strain in the Ge_xSi_{1-x} layer may enhance the channel mobility in the MOS device. It is a goal of this work to determine the effect of strain on carrier mobility in the channel region of n-channel and p-channel MOS devices.

FORMATION OF EPITAXIAL Ge_xSi_{1-x} LAYERS ON SILICON

The work which has been completed in the reporting period has concentrated on the formation of strained epitaxial Ge_xSi_{1-x} layers on silicon by ion implantation of germanium into silicon and subsequent wet oxidation of the Ge-implanted silicon. The feasibility of this method for forming device-quality Ge_xSi_{1-x} layers was investigated because of the widespread availability and relatively low cost of ion implantation (compared to chemical vapor deposition and molecular beam epitaxy).

Bare silicon wafers ((100) orientation, *n*-type, 5-10 ohm-cm) were implanted with 60 keV $^{70}Ge^+$ ions; the doses used were $5x10^{15}$, $1x10^{16}$, $2x10^{16}$, $4x10^{16}$, and $6x10^{16}$ cm^{-2}. The wafers were then oxidized in steam, so that the original implanted region of silicon was entirely consumed, and so that the germanium was "piled up" into a thin layer at the SiO_2/Si interface;

the oxidation temperatures ranged from 800°C to 950°C. The low diffusivity of germanium in silicon, coupled with the preferential segregation of the germanium into silicon (rather than silicon dioxide), leads to the formation of a distinct, germanium-rich layer of Ge_xSi_{1-x} at the oxidizing SiO-/Si interface; this Ge_xSi_{1-x} layer is epitaxially aligned with the silicon substrate.

Extensive physical and electrical characterizations were performed on the various wafers; in the following sections, the results of the characterizations are briefly summarized.

A. Physical Characterization Results

After the wet oxidation step, the silicon dioxide was examined under an optical microscope in the dark-field mode. The quality of the oxide was found to be poor, with noticeable pinholes; the density of pinholes increased with increasing Ge implant dose, and decreased with increasing oxidation temperature. The poor quality of the thermal oxide was confirmed by electrical measurements of the breakdown voltage. Clearly, this oxide is unsuitable for both field and gate applications; hence it would have to be stripped off and replaced by a deposited insulator.

In order to determine the effect of germanium on the oxidation rate of silicon, the thickness of the silicon dioxide was measured using an ellipsometer and also using a Nanospec interferometer. The ellipsometer and Nanospec measurements were in agreement to within a few percent. It was found that the Ge-implanted wafers oxidized more rapidly than a corresponding nonimplanted wafer, and that the enhancement in oxide thickness increased with increasing Ge-implant dose (for a given oxidation time and temperature) and decreased with increasing oxidation temperature (for a given Ge-implant dose and oxidation time).

In order to determine the thickness of the Ge-rich layers formed at the interface between the silicon substrate and the silicon dioxide, wafer samples were analyzed by cross-section transmission electron microscopy (XTEM). It was found that the thickness of the Ge_xSi_{1-x} layer increases with the implant dose, from 20 Angstroms for an implant dose of $5x10^{15}$ cm^{-2} to approximately 250 Angstroms for an implant dose of $6x10^{16}$ cm^{-2}, indicating that x is greater than 0.5 (assuming that none of the implanted germanium was incorporated into the silicon dioxide).

Transmission electron microscopy (TEM) was also used to characterize the defects associated with the Ge_xSi_{1-x} layer. For the samples which were implanted with a dose greater than or equal to $1x10^{16}$ cm^{-2}, the TEM results indicate that the Ge_xSi_{1-x} layer is inhomogeneously strained, due to local strain reductions via misfit dislocations located at the Ge_xSi_{1-x}/Si interface. The presence of misfit dislocations was verified by high-resolution electron microscopy (HREM). Stacking faults were observed in most of the samples,

increasing in density with increasing implant dose. Judging from the HREM photographs, nucleation of the stacking faults occurred at the Ge_xSi_{1-x}/SiO_2 interface during the oxidation step, possibly due to the presence of super-saturated interstitial silicon atoms at that interface. It is clear that, in order to obtain a uniformly strained layer of Ge_xSi_{1-x}, low implant doses (less than $1x10^{16}\,cm^{-2}$) must be used.

The interface roughness associated with the Ge_xSi_{1-x} layer was also studied by HREM. It was found that both the roughness of the SiO_2/Ge_xSi_{1-x} interface and the roughness of the Ge_xSi_{1-x}/Si interface increase with increasing implant dose, and with increasing oxidation temperature, with the Ge_xSi_{1-x}/Si interface roughness increasing more dramatically. The increasing roughness of the SiO_2/Ge_xSi_{1-x} interface with increasing implant dose may partially account for the observed increase in density of stacking faults with increasing implant dose, since surface roughness at the oxidation interface can facilitate the nucleation of stacking faults. Since surface roughness is also known to reduce the effective carrier mobility in MOS devices, the HREM results suggest that lower dose Ge-implants would be more desirable for MOS applications; however, the thickness of the Ge_xSi_{1-x} layer formed using a lower dose Ge-implant may not be large enough to have a significant effect on the channel conduction in an MOS device.

Secondary Ion Mass Spectroscopy (SIMS), using a primary beam of 10 keV oxygen ions, was used to analyze samples of various wafers. Because of matrix effects, it was not possible to accurately determine the absolute concentration of germanium in the Ge_xSi_{1-x} layer; in addition, because of "knock-on" and sputtering-induced roughness effects, the resolution of the SIMS method used is greater than 200 Angstroms, which made it difficult to accurately determine the shape of the germanium concentration profile. However, trends in the variations of Ge_xSi_{1-x} layer thickness and maximum germanium concentration can be determined by comparing the SIMS profiles of the Ge_xSi_{1-x} layers for various Ge-implant doses and oxidation temperatures. From these comparisons, it was found that both the peak germanium concentration in the Ge_xSi_{1-x} layer and the thickness of the Ge_xSi_{1-x} layer increase with Ge-implant dose, and do not vary with the oxidation temperature.

Rutherford Backscattering Spectroscopy (RBS) analyses were performed on various wafer samples using 2.4 MeV He^+ ions and a scattering angle of 170°. The depth resolution of the RBS method used is approximately 200 Angstroms. Since the thickness of the Ge_xSi_{1-x} layer in the various samples is (in general) smaller than the depth resolution of this analysis method, the distribution profile of the Ge once again could not be accurately determined; however, the integrated Ge dose in the Ge_xSi_{1-x} layer could be estimated from the peak concentration and half-width of the RBS profile, and was consistently found to be slightly greater than the implanted dose. Also, to within the detection limits of RBS, no germanium was detected in the silicon dioxide. It can be concluded, from the RBS analyses, that no germanium was lost to

the silicon dioxide during the oxidation step. Comparison of the RBS profiles for various Ge-implant doses and oxidation temperatures confirmed the variation trends in peak germanium concentration and Ge_xSi_{1-x} layer thickness observed by SIMS.

B. Electrical Characterization Results

After the wafers were oxidized in steam, pure aluminum was sputtered on and patterned to form circular gates for capacitance vs. voltage (C-V) measurements, and the wafers went through a subsequent forming-gas anneal. For the capacitors on each of the wafers, the Fermi level in the substrate was "pinned", so that the capacitance essentially did not vary with voltage. This "pinning" effect may be due to electrically active defects associated with the stacking faults which are known (from TEM) to be present in the Ge_xSi_{1-x}/Si substrate. Also, from oxidation studies of Ge_xSi_{1-x}, C-V measurements have shown that oxides on Ge_xSi_{1-x} have high negative fixed charge and high interface trap density, both around 10^{12} cm^{-2} [LeGoues] [Margalit] [Neugroschel]. It is quite possible that the entire (*n*-type) surface of the Ge_xSi_{1-x}/Si substrate is simply inverted in all of the wafers in this work.

ELECTRICAL EFFECTS OF Ge AT THE Si/SiO_2 INTERFACE

In order to study the electrical effects of germanium at the Si/SiO_2 interface, a series of low-dose germanium implants were performed on a new set of silicon wafers ((100) orientation, *n*-type, 8 ohm-cm). The implant energy was 40 keV, and the implant doses ranged from $1x10^{11}$ to $1x10^{14}$ cm^{-2}. Again, the implanted wafers were oxidized so that the implanted region of the silicon was consumed, and so that the germanium would be piled up at the SiO_2/Si interface. The oxidation temperatures which were used were 900°C and 950°C. Because the resulting concentrations of germanium at the SiO_2/Si interface are too low to be accurately detected by physical characterization methods, no physical characterizations were performed on these low-dose wafers. Pure aluminum was sputtered onto the oxide and patterned to form gates for C-V measurements, and the wafers were subsequently annealed in forming gas.

Measurements of the oxide fixed charge (N_f) and interface trap density (D_{it}) were obtained from C-V measurements on the low-dose Ge-implanted wafers. The presence of germanium at the SiO_2/Si interface was found to have no effect on the fixed charge -- N_f remains positive, does not vary significantly with Ge-implant dose, and is no higher for a Ge-implanted wafer than for a nonimplanted wafer; however, the presence of germanium at the SiO_2/Si interface was found to affect the interface trap density: D_{it} is noticeably affected by the presence of germanium for interface concentrations greater than $1x10^{13}$ cm^{-2}, which corresponds to approximately 1 atomic percent germanium in silicon at the oxide interface. The interface trap density increases rapidly with increasing germanium interface concentration, to approximately $1x10^{11}cm^{-2}eV^{-1}$ for an interface concentration of $1x10^{14}$ cm^{-2}, which corresponds to

approximately 10 atomic percent germanium in silicon at the oxide interface.

From this low-dose Ge-implant study, it would seem that the presence of germanium at the SiO_2/Si interface only affects the interface trap density, and not the fixed charge density at the SiO_2/Si interface. The high negative fixed charge densities observed for oxides on Ge_xSi_{1-x} may be due to acceptor-like defect states introduced at or near the SiO_2/Si interface by misfit dislocations and stacking faults.

Ongoing Work

Further experiments are currently being conducted in order to determine the optimum conditions for the formation of device-quality Ge_xSi_{1-x} layers by the implantation/oxidation technique. The viability of other techniques based on ion implantation of germanium for forming device-quality Ge_xSi_{1-x} layers is also being investigated. In addition, in order to assess the advantages of strained Ge_xSi_{1-x} layers for MOS applications, experiments are being planned for fabrication of MOS devices on silicon wafers which have epitaxial CVD Ge_xSi_{1-x} layers .

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Unit: 9

TITLE: Combined Equalization and Coding

PRINCIPAL INVESTIGATOR: J.M. Cioffi

GRADUATE STUDENTS: J. Aslanis, G. Dudevoir, J. Tu, J. Chow, R. Ziegler and H. Bims

GRADUATE STUDENTS: S. Kasturia, A. Ruiz and P. Fortier

Scientific Objectives:

Our objective continues to be the design of combined coding and equalization methods for channels with severe interstymbol inteference and crosstalk. Our work during the past year has produced much new fundamental theory of the solution of this problem, as well as developing and understanding of computational requirements and complexity of the methods that we have developed. We have also looked at both equalization and coding issues in the area of wideband digital mobile data transmission.

Summary of Research:

In the area of fundamental understanding of the combination of equalization and coding, we have developed some additional methods that will also achieve the same performance levels as our original vector coding work that was reported last year. We have also looked at methods to improve vector coding, namely block equalization and precoding methods, fast fourier transform based coding, and a constellation shaping method for vector coding that we call the shell construction. We have also studied in much greater detail the application of these methods to the High-Speed Digital Subscriber Loop (HDSL) that is currently under study for standardization within the American National Standards Institute. Because of the applied nature of this latter work, Bellcore and AT&T have both funded this work, and as well, another company is seriously considering joining them. Thus, the JSEP funds were used to seed this area of research which is now nearing independent funding. We, thus, have also used JSEP funds to seed research in another area, that of digital wideband mobile radio, and have fundamental theoretical (and simulation) results on equalizer tracking in the presence of severe multipath fading and have extended some of our previous coding work to the case of the continuous phase modulation that is attractive in wideband mobile networks.

1. Fundamentals of Combined Equalization and Coding:

Two papers reported as submitted last year have been appropriately modified and accepted for publication [Kasturia 90] and [Ruiz 90]. The first paper was the introduction of the Vector Coding concept and a detailed analysis of its importance. New results in the final form of that paper describe how the optimal cut-off rate performance of vector coding can be extended back to improve some more traditional methods of modulation, like decision-feedback equalization, when appropriately combined with spectral shaping and coding concatenation. A more detailed discussion of this finding explicitly for the so-called Tomlinson Precoded form of decision feedback will be reported in the conference paper [Cioffi 89]. The second paper [Ruiz 90] studies a reduced complexity form of vector coding that we call "discrete multitone" modulation. This method achieves the same gains as the original vector coding method, but with considerably less computation (which we will discuss more in connection with HDSL in the next section).

Another two conference papers [Kasturia 88], [Kasturia 89] report on a new block-structured equalization method that can be used to reduce the complexity of the original vector coding methods. The first paper [Kasturia 88] describes what we call a "Block Decision Feedback Equalizer" and it eliminates the long block length and "zero-stuffing" features of the original vector codes, which are a problem in practical implementation. This structure coincidentally also solved a long-standing problem in high-speed implementation of decision-feedback equalizers, namely the difficulty in pipelining the computations because of the dependency on previous decisions. This work was described in [Cioffi 88]. The second block equalization paper [Kasturia 89] introduces the concept of block Tomlinson Precoding, which allows the combination of shaping and coding gain to be realized with a Tomlinson Precoder, which was impossible prior to that concept. This method has been recently generalized and improved in a series of papers by Eyuboglu and Forney of Codex, into what they call "Trellis Precoding" [Eyuboglu 90].

We have also found a way to append shaping gain to vector coding methods, when coding must be performed within one block interval because of delay contraints. This method is called the "shell construction" and is described in the submission by Fortier [Fortier 89].

We have developed a proof that the vector coding methods can be used to achieved the so-called cut-off rate, the maximum theoretically achievable rate with finite complexity, in the presentation by Aslanis [Aslanis 90]. We have also found a way to extend vector coding gains by using a "mean-square vector coding" method that does not completely eliminate interference between parallel subchannels, but rather achieves the highest possible signal-to-interference ratio on each channel, as described in the presentation [Cioffi 90].

2. High-Speed Digital Subscriber Line Application:

We have now studied the digital subscriber loop application in greater detail than previous reports. The objective here is to achieve a data rate of approximately 1.5 Mbps over twisted pair channels (i.e.. those that constitute the last "mile" - up to 12 kft - in the telephone network). While this is a difficult channel in that on worse-case channels the cutoff rate just barely exceeds 1.5 Mbps, we have been able to develop in theory an off-line simulation cost-effective systems that can achieve these rates. The present system under study is shown in Fig. 9.1. This system is described in terms of performance in two invited conference papers in [Tu 89] and in terms of reduced computational requirements [Chow 90]. As well, a theoretical justification, which includes an extension of some of the original shannon capacity results to channels with cross-talking interference, of some of the choices in this system was presented in the invited conference paper by Aslanis [Aslanis 89].

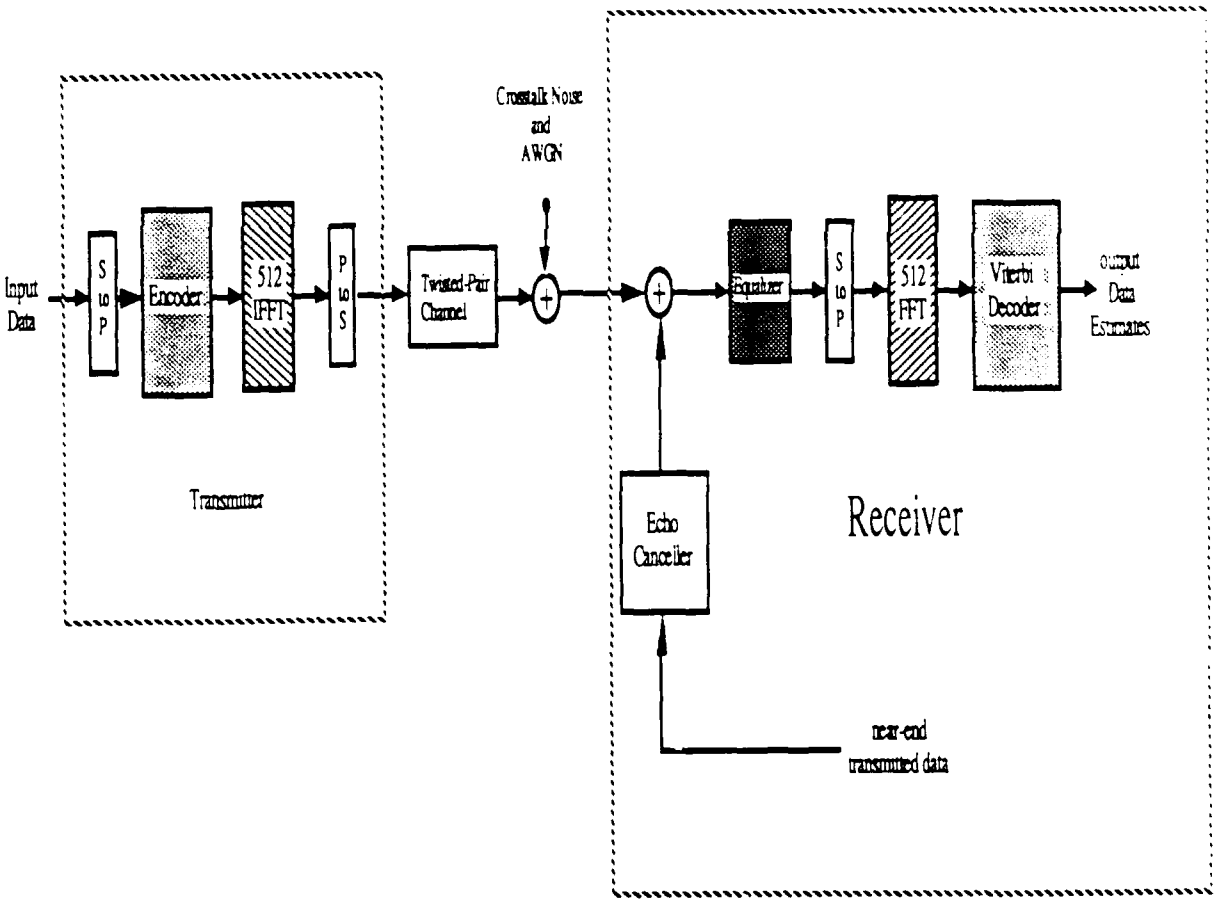

Figure 9.1

Work continues on the HDSL application in the areas of crosstalk coding strategies, adaptive equalization method and intialization protocol, echo cancellation, and a high-speed programmable detector chip designed to facilitate the implementation of the Viterbi Decoder(s) that will be necessary in the present system.

3. Digital Wideband Mobile Radio:

As mentioned earlier, we have also begun serious studies of wideband digital mobile radio transmission. Both Europe and the United States have recently elected to change their present analog cellular telephone, networks to digital replacements. Our work has been oriented towards increasing the transmission rate on the mobile link, which thus allows a more efficient use of the scarce existing spectrum for this service. Of primary interest to us here is the problem of multipath fading, which can lead to both frequency-selective and shadow fading in these networks. In the case of rapidly time-varying frequency selective fading, we will present the paper by Ziegler [Zeigler 89] that deals with the relative ability of several popular adaptive equalization algorithms to track multipath fades. Additionally, channels that are subject to flat fading (shadow fading) often use signal constellations that are within the class of modulation known as continuous phase. The continuous phase constraint induces restrictions on the modulation process that are analagous to those that we studied (with vector coding) in the intersymbol interference case. We have been able to successfully concatenate trellis codes with continuous phase modulation to develop a new class of CPM with coding gains significantly higher (few dB or more) than any previously reported, as described by Bims in [Bims 89].

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2. P. Fortier, "Multidimensional Signal Set Design for Transmission Over Parallel Channels", Dissertation, Department of Electrical Engineering, May 1989.
3. S. Kasturia, "Vector Coding for Digital Communications on Spectrally Shaped Channels", Dissertation, Department of Electrical Engineering December 1988.

Unit: 10

TITLE: Real-Time Statistical Signal Processing

PRINCIPAL INVESTIGATOR: T. Kailath

VISITING SCHOLARS: L. Godara

RESEARCH ASSOCIATES: R. Roy

GRADUATE STUDENTS: D. Slock, G. Xu and B. Ottersten

Scientific Objectives:

During the last nine months, progress in the area of sensor array processing has been concentrated in two areas:

1. extensions of the ***ESPRIT*** algorithm to wide-band signals,
2. developing and analyzing stable, fast algorithms for various adaptive beamforming applications.

The purpose of this report is to summarize the results obtained over this period.

Summary of Research:

A. Wide-band Array Processing via Spectral Smoothing

Various signal subspace algorithms have been recently proposed in the area of high-resolution narrow-band direction-of-arrival (DOA) estimation, e.g., **MUSIC** and ***ESPRIT***. The difficulty in extending these approaches to wide-band array processing essentially lies in the fact that wideband data doesn't fit the low-rank data model as does narrow-band data. The key point is there is no underlying signal subspace. Recently, several approaches have been suggested to resolve this problem including a spectral-spatial approach, the coherent signal-subspace method, modal decomposition algorithms and wide-band ***ESPRIT***. Each of these algorithms has one or several of the following shortcomings:

1. high computational cost,
2. inappropriate signal model assumption,
3. requirement for initial DOA estimates and complete knowledge

of array manifold.

During this reporting period, we have proposed a new and more efficient approach for estimating DOA of multiple wide-band sources via *spectral smoothing*. The method is comprised of the following basic steps:

1. time domain to frequency domain transformation (i.e., FFT),

2. spectral domain processing involving spectral *smoothing* of a nonlinear function of the transformed data chosen to enhance an underlying invariance structure designed into the array of sensors leading to pseudo-measurements with a model equivalent to the narrowband data model,

3. and subsequent application of narrowband techniques such as ***ESPRIT*** and **MUSIC** for obtaining DOA estimates of the broadband sources.

The suggested algorithm requires much less computation than the existing approaches and does not require complete knowledge of the array manifold. Initial DOA estimates are not required, nor is a specific signal model (e.g., ARMA) assumed. Currently, however, the signals must be *spectrally uncorrelated*, a condition that holds, for example, if the individual signal spectra are non-overlapping.

In preliminary results obtained to date, the proposed approach has outperformed previous techniques, as evidenced by computer simulations. A limited amount of analysis has also been performed employing simplifying assumptions. Papers on this approach are currently in preparation, one of which [Xu] has been accepted for presentation at this year's SPIE conference. More detailed performance analysis is currently ongoing. Efforts are in progress to further exploit spectral properties of certain type of signals, e.g., cyclostationary and other modulated signals.

2. Modular and Numerically Stable Fast Transversal Filter Algorithms for Adaptive Beamforming

A beamformer is a processor used in conjunction with an array of antennas or sensors to provide a form of spatial filtering. The sensor array collects spatial samples of propagating wave fields, which are processed by the beamformer. The objective is to estimate the signal arriving from a desired direction in the presence of noise and interfering signals. A beamformer performs spatial filtering to separate signals that originate from different spatial locations.

In its simplest form, the beamformer output at time T, y(T), is given by a linear combination of the data at the p sensors at time T:

$$y(T) = \sum_{i=1}^{p} w_i x_i(T) \ .$$

This form is appropriate for so-called narrowband beamforming where all signals of interest are assumed to have basically a single temporal frequency component.

In adaptive beamforming, the objective is to adjust the weights so as to reconstruct the *desired* signal and reject all others leading to a standard regression problem. The LMS and RLS algorithms are two basic algorithms for adjusting the weights in the regression problem. The LMS algorithm attempts to minimize the stochastic mean square of the error signal and does so by employing a steepest-descent algorithm with an instantaneous estimate of the gradient vector. In contrast, the RLS algorithm minimizes at all times a deterministic least-squares criterion. The advantages of RLS algorithms over LMS algorithms in aspects such as convergence speed and tracking behavior are well-known.

However, in practice the use of LMS algorithms is widespread due to its computational simplicity. More recently, fast RLS algorithms (fast transversal filters (FTF) and fast lattice algorithms (FLA)) have been introduced that circumvent the computational burden of the Riccati equation in the conventional RLS algorithm.

C. Numerically Stable FTF Algorithms

The LMS and the conventional RLS have been found to be exponentially numerically stable.[1] For a while, it was generally assumed that the FTF algorithm was inherently numerically unstable and that no stable FTF algorithm existed that could solve the exact RLS problem. This was recently disproved in [Slock 88], [Slock (b)] [Slock (c)]. The solution to the stability problem in FTF algorithms involves two key ingredients: redundancy and error feedback. Nontrivial redundancy can be introduced in the FTF algorithm in the sense that certain quantities can be computed in two fundamentally different ways. This redundancy makes certain measurements of the numerical errors available. These measurements can then be fed back to modify the dynamics of the numerical error propagation. It turns out that the feedback coefficients can be chosen so as to stabilize the error propagation.

Other techniques for improving the performance of narrowband adaptive beamformers at reduced computational cost were also investigated. In [Godara (d)] and [Godara (b)], structured gradient LMS algorithms were proposed and analyzed. The idea is exploit some known structure of the asymptotic statistics (covariance) of the array output to obtain

improved estimates of the second order statistics, which in turn lead to improved estimates of the *optimal* weights. For example, the output covariance is Toeplitz if a uniform linear array is immersed in an uncorrelated signal and noise environment. Imposing this structure leads to a gradient algorithm that is less sensitive to errors in the look direction as demonstrated by analysis and simulation results.

D. Modular Multichannel FTF Algorithms

The broadband beamforming application involves the multichannel formulation of the FTF algorithm. The conventional multichannel FTF algorithm requires matrix operations. Because of these matrix operations, both the simplicity and the relatively high throughput of single-channel algorithms are sacrificed in those multichannel implementations. The difficulties in implementation of multichannel algorithms have spurred a growing interest in *scalar* implementation of multichannel recursions, namely implementations that require no matrix processing. Moreover, the increasing interest in dedicated VLSI hardware implementation favors algorithms that can be implemented in *modular architectures* with a regular and highly parallel structure.

In [Slock 89], [Slock], a geometric modular decomposition principle has been applied to arrive at a new multichannel FTF algorithm in which the p channels are processed *sequentially* i.e., one at a time). In FTF algorithms, the fast updating of the Kalman gain involves an order update and an order downdate. In the conventional multichannel FTF algorithm, these up/downdates are done in block form for all channels simultaneously. The modular decomposition principle, however, dictates that these updates and downdates be performed for each individual channel sequentially. This decomposition leads to a modular architecture consisting of regularly interconnected simple processing blocks that perform scalar operations. Using O(p) parallel processors, the beamformer throughput can be increased by a factor p.

E. Broadband Adaptive Beamforming

Often in adaptive beamforming, the signals involved have a broadband temporal frequency spectrum, or they are comprised of multiple narrowband components. In such situations, a broadband beamformer will be more effective in separating the desired signal from interferences. This is so since a broadband beamformer not only exploits differences in spatial angles, but also differences in temporal frequency content to separate different signals. A typical broadband beamformer implementation has a tapped-delay-line at the output of each sensor. The beamformer output in this case can be expressed as

$$y(T) = \sum_{i=1}^{p} \sum_{k=0}^{N-1} w_{i,k} x_i(T-k),$$

where N is the number of delays in each of the p sensor channels. Again the objective is to obtain weights that pass a given signal and reject all others.

In general, multiple linear equality constraints can be employed for added control over the beampattern. The least-squares problem subject to linear equality constraints that thus arises can easily be transformed into an unconstrained least-squares problem. This unconstrained problem will be of a reduced dimensionality and involves a number of tapped-delay-lines that is equal to the number of sensors minus the number of linear constraints employed. It has been shown that the equivalent unconstrained problem can still be solved recursively in time using the modular multichannel FTF algorithm (see [Slock (a)].

Also in the area of broadband adaptive beamforming, development and analysis of postbeamformer interference canceler (PIC) structures were undertaken. The basic idea is to reduce the computation load by first reducing the data to a statistic of smaller dimension (than the number of sensor elements) and attempt to optimize some performance criteria in the reduced dimension. For example, from a multi-element sensor array, two *beams* can be formed by using two sets of weights that *steer* the antenna toward a desired look direction and elsewhere. The objective is then to find an optimal weight for combining these two scalar outputs to optimize say the output signal-to-noise ratio (SNR).

For broadband signals, the weights must also include steering delays, and the design parameters are several weights in a tapped-delay line filter for processing the *interference beam* output. When a minimum output power criterion is used, however, a significant amount of signal cancellation results when the signal component is present in the interference channel. In [Godara (a)] and [Godara (c)], a frequency domain PIC structure was proposed and analyzed. Methods for reducing the sensitivity of the algorithm to the bandwidth of the sources were suggested, and the dependency of the PIC performance on the choice of coordinate system was investigated. The features of the proposed approach include:

1. need for steering delays eliminated in the frequency domain PIC (FDPIC),
2. capability of specifying the frequency response of the FDPIC in the look direction,
3. adaptive adjustment of the interference channel weights
4. independence of coordinate system origin even in presence of various antenna pattern constraints.

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